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COMPUTERS AND DISPLAYS/CONTROLS
STATE-OF-THE-ART TECHNOLOGY STUDIES

Prepared For

Joint Army/Navy Aircraft-Instrumentation Program
Integrated-Cockpit Research Program, Contract Nonr-4951(00)
Distribution of this Report is Unlimited

Prepared By

D. J. Pizzicara

February 1966

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LITTON SYSTEMS, INC.
Guidance and Control Systems Division
5500 Canoga Avenue, Woodland Hills, California

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ABSTRACT

Computers and Displays/ Controls for avionics systems are discussed primarily from a technology standpoint. The current state of the art is reviewed, current research developments are pointed out and a prediction of when these developments will be incorporated into avionic systems is given.

Section II of this technology report is devoted to computers and has the following major categories: a) Logic, b) Memory, c) Computer Organization, d) Analog/Digital Conversion.

Further details on the Computer section of the report are:

1. Logic. A brief statement of system requirements is presented. The current technology, including monolithic-silicon integrated circuits and thin-film hybrids (thin-film passive components with semiconductor active elements), is extensively reviewed. Future technology, including Metal-Oxide Silicon (MOS), batch-fabricated monolithic bipolar arrays, and pure thin-film developments are assessed. Developments in MOS and bipolar silicon arrays has been rapid in contrast to only slow progress in thin-film active devices. Thus the prediction is made that monolithic silicon in unipolar and bipolar forms will pre-empt the field of logic circuitry up to and including the 1973-78 time period.
2. Memory. System requirements are discussed and ideal memory characteristics presented. Current NDRO memories for avionics are reviewed, including multiaperature ferrites (MAD), BIAx, THIN FILM, ROPE. DRO memories including core types and films are also presented. Research in advanced memory techniques is presented, including the waffle iron, MOS memories, ferrite laminates, the flute memory, and the SMID. These techniques are all based on "batch-technology fabrication". However, continuing progress in cores indicates that such memories will be in use for many years. The ferrite laminates are currently the most vigorous challenger and should be considered for any new avionics computer.

3. Computer Organization. Advantages of functionally modular computer systems for avionics include versatility, growth capability, programming ease, and logistics and maintenance. The impact of complex logic chips leads to so called block-oriented systems having, for example, 10×10 arrays of computing elements. Contemporary organizations are assessed for suitability to block-oriented computer systems. Disadvantages of DDA and ~~conventional~~ general-purpose organizations indicate a need for new logic organizations, such as the Solomon or Dinary types.
4. A/D Conversion. Interface and conversion requirements are illustrated for three different avionic systems. These are classified in three categories as a function of data rate requirements. Present day conversion techniques are reviewed, including shaft encoders of various types, ladder networks, the successive approximation technique, and several synchro-to-digital and digital-to-synchro techniques. A summary of converter characteristics is given in table form. Progress in advanced conversion systems is reviewed. This includes direct-digital-outputting transducers, thin-film ladders, miniaturization of optical shaft encoders, neo-magnetic and nuclear radiation types. Hall generator devices are also discussed; however, poor potential is forecast.

The section devoted to Displays/Controls (Section III) has the following major categories: a) CRT's, b) Scan Conversion, c) Color, d) Analog/Digital Techniques, e) Electroluminescence.

With respect to the Displays/Controls, the following is a summary for each of the principal topics reviewed:

1. CRT's. General-purpose types, including electrostatic, magnetic, dual deflection, and multi-gun, are discussed and tabularized. Special-purpose CRT's of the following types are reviewed: optically ported; beam shaping; character generation; projection; the Kaiser-Aiken thin CRT; storage tubes; and recording and printing types. Improvements in ruggedness, resolution, brightness, and reduction in cost will prove the CRT difficult to beat until well into the 70's. One possible competitor is electroluminescence.

2. Scan Conversion. The theory of scan conversion, including single- and dual-gun types is extensively reviewed. Scan-conversion tubes for avionics displays must currently be regarded as developmental. However, rapid progress is being made with regard to ruggedization and reduction in volume so that these devices should be in considerable usage by 1969-1970 time frame. The introduction of scan conversion will facilitate the utilization of a wide variety of sensors. A competitive technique for avionics is the multinode, rapid erase storage tube.
3. Color. Four methods of obtaining color displays are: a) evacuated tubes; b) solid state; c) liquid; d) gas. Of these, the CRT is by far the most widely used at this time and will remain so indefinitely in the foreseeable future, barring a major breakthrough in an entirely new display technique.

Seven types of color tubes are reviewed and the conclusion is drawn that the following have the highest potential for utilization to provide a small screen display in color: (a) Shadow mask; (b) Aiken-Geer thin type, flat tube; (c) Lawrence Chromatron. Considerable development work is in progress, thus enhancing the prospect of using color displays in avionics systems by 1970.

4. Analog/Digital Techniques. The advantages of digital over analog range scaling are presented. These include perfect registration and reduction in noise sensitivity. Additionally the need for precision clamps is eliminated since the selection for display of sweep or synthetic data can be made digitally. Techniques for generating digital sweep are presented and difficulties with high clock speeds at short ranges is discussed (at 2 miles, $f_{\text{clock}} = 21.3 \text{ mc/s}$).

Analog vs digital generation of symbology is reviewed, including line generation by an analog integrator vs. digital sweep and symbol generation via lissajous, stroke, or dot-pattern techniques.

5. Electroluminescence. Application of EL displays in the cockpit, together with system requirements is presented. EL state of the art is reviewed for the following topics: fabrication techniques; phosphors; panel design; storage requirements; and addressing and drive problems.

Advances required in the state of the art to expand the use of EL in the cockpit are presented. These include increased display legibility, longer life, and higher resolution. Potential solutions to improved legibility are increased brightness, and contrast enhancement techniques, with current emphasis on the latter. The improvement of life and resolution are basic material problems.

System problems presented by computer-driven and scanned EL displays also require solution. Among these are the requirement for a low cost data buffer between the computer and the display to keep I/O traffic within reasonable limits. Selection and drive techniques for the EL panel also require further development. The requirement for shades of grey in the situation displays imposes a further restriction on techniques to drive the EL. At this time it appears that the ceramic ferro-electrics offer the best hope for a batch-fabricated device combining the desired properties of selection and variable drive.

This review concludes with a system description of a 10" x 10" thin-film panel together with associated data buffer, drive circuitry, and interface electronics. Using data derived from "off the shelf" avionics components, we have included estimates of size, weight, volume, and power.

The work reported herein was performed by the following personnel:

D. J. Pizzicara:	Section 2. 1, 2. 2, 2. 3, 2. 4, 3. 2, 3. 5, overall editing and organization.
H. C. Martin:	Section 3. 1, 3. 3, 3. 4, 3. 6
J. O. Campeau:	Sub-section 2. 3. 8

I INTRODUCTION

The objective of the Integrated Cockpit Research Program is to achieve an optimal synthesis for a hypothetical aircraft system, circa 1973-78. This program will use the most advanced technology projected for this period in order to unburden the pilot and copilot. From these efforts, the integrated cockpit derived will be characterized by maximum man-machine optimization in terms of the technological capability of the advanced time frame.

A starting point for the advanced-avionics-technology projection is a detailed examination of the current state of the art in computers and displays. The assumption made is that the "art" will follow the evolutionary patterns of the last 10-15 years, thus permitting a rational approach in projecting to the future time frame. The information base so derived will be highly useful in the examination of the other key technologies associated with avionics due to their intimate dependency on computing techniques and microelectronics.

With the technology-base established, an ultimate goal of the Integrated Cockpit Research Program can be achieved: complete automation of the cockpit. This implies the ability of the machine to express judgments, make decisions, and perform control actions, albeit monitored by the crew. Other candidate systems will be derived that will use progressively less automation, i. e., man is allocated successively-augmented command and control functions. Cost/effectiveness methodology will be applied to ascertain systems realizable in the 1973-78 period taking into account performance, physical characteristics, cost, etc.

This rationale is suggested by the increasing proliferation of equipment in avionics systems. A typical example of this trend is provided by the advanced V/STOL, US-FRG now in the specification phase. Among the avionics included for this aircraft are the following:

1. Communication: UHF-VHF radio; UHF emergency radio; HF-SSB transceiver; HF-VHF transceiver, secure communications including direction finding and DME.
2. Forward-looking sensor group for TF/TA, ground mapping, air-to-air search, air-to-ground ranging.
3. Navigation: Inertial; LORAN C and D; TACAN; ADF.
4. Mission and traffic control:
 - All-weather instrument landing
 - IFF/SIF/AIMS
5. Data Link - air/air, air/ground
6. Reconnaissance sensors: SLAR, IR mapper; camera system; Down-ward looking airborne radar
7. Warning systems - ELINT; IR

The probabilities are that the 1973-1978 avionic suit will be at least as complex.

This example is indicative of the magnitude of the cockpit integration task now facing the avionics system designer. Central to this integration is the role of the computer complex and displays/controls. Through these integrative systems, the many avionics are utilized and controlled. The degree of system effectiveness achieved is in large part dependent on the adequacy of the computer-display complex.

In the material to follow, the key aspects of avionics computer systems will be examined. Emphasis is placed on logic elements, memory, computer organization concepts, and input-output conversion systems. Current research trends seeking to advance the state of the art will be described. From these examinations, a projection will be drawn of the avionic computer capability as existing in the 1967, 1969-70, and 1973-78 time frames.

With respect to displays/controls, a similar approach is taken. The primary vehicles for current avionics displays are the CRT and electro-mechanical instruments. Increasing sophistication of these systems through application of scan conversion, electroluminescence, color tube,

and advanced storage tubes is assessed. Additionally, the increasing use of digital techniques for sweep and symbol generation are reviewed. A projection for the cockpit display capability for the 1967, 1969-70, and 1973-78 period will be made.

II COMPUTERS

2.1 LOGIC

This section of the technology report will review the state of the art of present-generation digital circuits and examine the more prominent developments currently in the developmental stage.

In this report we shall be concerned only with integrated logic circuitry. The era of discrete logic components is at an end, as may be seen by the computer developments in progress in both the IHAS and ILAAS programs, as well as antecedents such as Minuteman and Phoenix. Motivation for these programs came from recognition of the unique advantages of integrated circuitry in reliability enhancement, size, weight, power reduction, and cost reduction. These advantages have resulted in acceleration of integrated circuitry to the extent that currently-produced avionics computers are 90-percent device integrated. The typical state-of-the-art avionics computer occupies less than a 3/4 cubic foot of volume, weighs about 30-50 pounds, contains up to 32,000 words of random-access storage, and computes at a rate in excess of 100,000 operations per second. Yet, even these capabilities will appear antiquated when the goals of current research are realized.

2.1.1 System Requirements

The requirements that must be fulfilled by elementary digital circuits for avionics computers are:

- Performance of a basic logic function
- Ability to be interconnected to form complex logic networks, and
- Sufficient operating speed.

The logic functions performed may be any of the several equivalent Boolean sets: AND, OR, INHIBIT; AND-NOT (NAND); OR-NOT (NOR); etc. Interconnection of the elementary logic functions into complex logic

networks permits the realization of the various types of digital computers. To permit such interconnection, the logic circuit must possess several attributes: First, the circuits must be characterized by a sufficient degree of isolation so that one circuit may drive many circuits and may also receive inputs from a multiplicity of circuits. Secondly, the input-output signal levels must have a large degree of compatibility to facilitate interconnectability. With respect to speed, the constraints are the performance of the real-time control as required by avionics system. However, specific speed requirements are dependent on the actual organization of the computer i. e. serial vs. parallel, general purpose vs. digital differential analyzer, etc.

The logical properties of the elementary digital circuit are derived from the discrete-signal quantization provided. This is illustrated by the input/output transfer characteristic shown in Figure 2-1. The threshold value of the circuit is X_T . Input signals less than X_T are quantized to the X_1 level whereas input signals above X_T are quantized to the X_0 level. The quantization levels X_1 and X_0 are used to represent the binary logic equivalents 1 and 0 (note: these are not numerical values).

An important fact about the elementary digital circuits used to form logic networks is that they are not precisely identical. This implies that rather than a single threshold, 1, and 0 levels, a zone for each of these will exist. The threshold zone represents uncertainty as to the signal convergence and must be suitably restricted by imposition of tolerance parameters on the digital circuit. Specifically, to assure binary quantization, the threshold zone must not extend into the range of the 0 and 1 signals.

The imposition of suitable circuit tolerance parameters is the chief problem in the design of the elementary logic circuit. Consideration must be given to many variables, including the variation of device parameters as a function of environmental changes and aging; the variation of device quantization levels as a function of the number of inputs driving the circuit and the number of outputs which must be driven (fan in and fan out); and the effects of noise. The tolerance parameters ultimately selected represent a tradeoff between performance criteria and cost criteria. The latter are determined directly by the effect of parameter tolerance selection on circuit production yields as well as power dissipation.

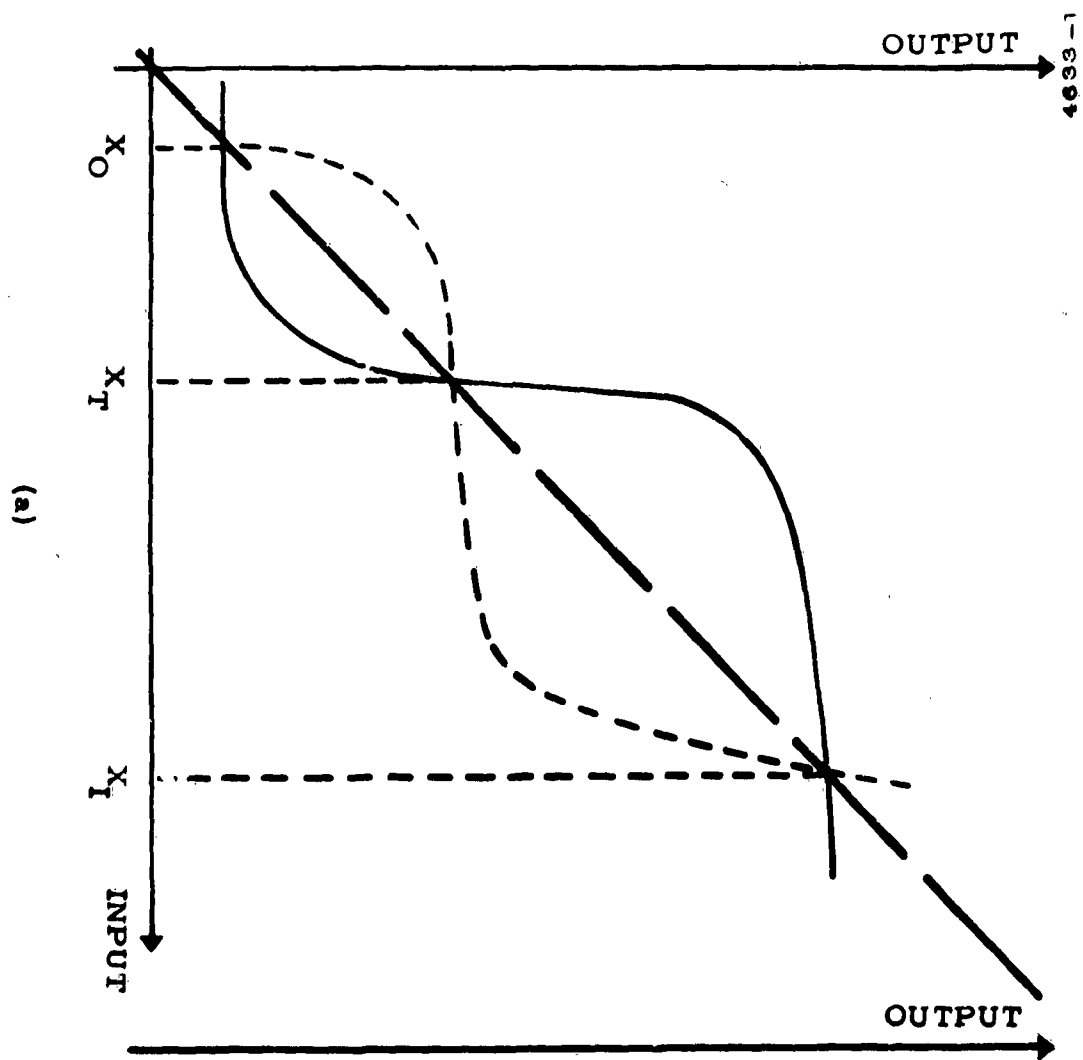


Figure 2-1. Input-Output Relation

2. 1. 2 State of the Art in Logic Circuitry

Present generation electronic digital circuits are predominantly based on the so-called "monolithic" silicon technology wherein all the components of the circuit are derived from the bulk silicon properties. A second type, which has received more limited application, is based on the use of discrete silicon transistor and diode chips connected with thin film passive components. This is the so-called "hybrid" approach. In either case, the circuits are fabricated in planar configurations with multilayer interconnecting techniques utilized.

Monolithic Integrated Circuits

The term "monolithic integrated" connotes that the entire logic circuit is formed in a single-crystal chip of semiconductor. The circuit's components, active and passive, and the required interconnections are made by a series of photolithographic and diffusion steps. This increased functional utilization of the bulk silicon properties has been achieved through the following: improvements in materials processing; the realization of resistive and capacitive components from the bulk semiconductor; and the achievement of electrical isolation between the elements of the circuit separated only by a few mils.

1. Epitaxy and Planar Processes

The process improvements that are most important to integrated circuits are epitaxy, the planar technique, and photolithography.

Epitaxy is the growth of single-crystal semiconductor on a substrate, the growth exhibiting the same orientation as the substrate. The standard silicon epitaxy is achieved through the reduction of silicon tetrachloride by hydrogen. Following epitaxy, p-n junctions and passive components are fabricated by diffusion through the epitaxial layer. In addition to achieving higher carrier mobility (hence active devices with superior gain characteristics), epitaxy, when combined with the planar process, permits the achievement of multiple p-n junctions and passive components in the same chip (of lengths and widths measured in mils). The planar process utilizes a thermally grown silicon dioxide layer to passivate the semiconductor surface. Subsequent etching of the surface layer is performed to permit diffusing further n- or p-type layers which constitute the circuit elements or parts thereof.

2. Photolithography

Along with the improvements in the semiconductor material processes, accurate geometry control is required via photolithography. The steps in photolithography consist of coating with a photo-resist material, exposure by contact printing through a photomask, and subsequent removal of the unexposed oxide. The dimensional tolerance to which this is accomplished directly affects transistor characteristics (principally f_{max} , the maximum frequency of oscillation) as well as the accuracy of the remaining circuit elements. Tolerances to 1/3 mil are routinely achieved. Extending monolithic circuitry techniques to produce entire logic functions such as a shift register in a single chip requires that tolerances be further reduced to 0.1 mil and less. Such accuracies are beyond the capability of conventional optical systems with the result that electro-optical techniques are being explored.

3. Isolation Techniques

Monolithic transistor geometry differs from its discrete counterpart as shown by Figure 2-2. The geometric configuration is derived from the necessity for achieving isolation between the transistor and other circuit components. Isolation is achieved by the diffusion of p-type impurities through the epitaxial layer into the substrate thereby forming reversed biased p-n junctions. The junction exhibits resistance values in the order of hundreds of megohms. Unfortunately, the isolation junction also exhibits parasitic capacitance, which heretofore has limited logic speeds.

Two methods of reducing the effects of parasitic capacitance, in order of consideration, are: (1) through the use of buried layers; (2) through the formation of adjacent islands of single crystal silicon isolated from each other by an insulating layer of oxide. The buried layer technique has been achieved while the isolation island technique is under intensive investigation. Figure 2-3 shows the buried layer configuration. Basically, the low resistivity buried layer permits increasing the resistivity of the collector, which results in lower capacitance values. The penalty of increased saturation resistance is avoided, however, because the collector sheet resistance is in effect shunted by the low buried layer resistance. With this technique the monolithic transistor achieves performance approaching its discrete counterpart, see Table II-1.

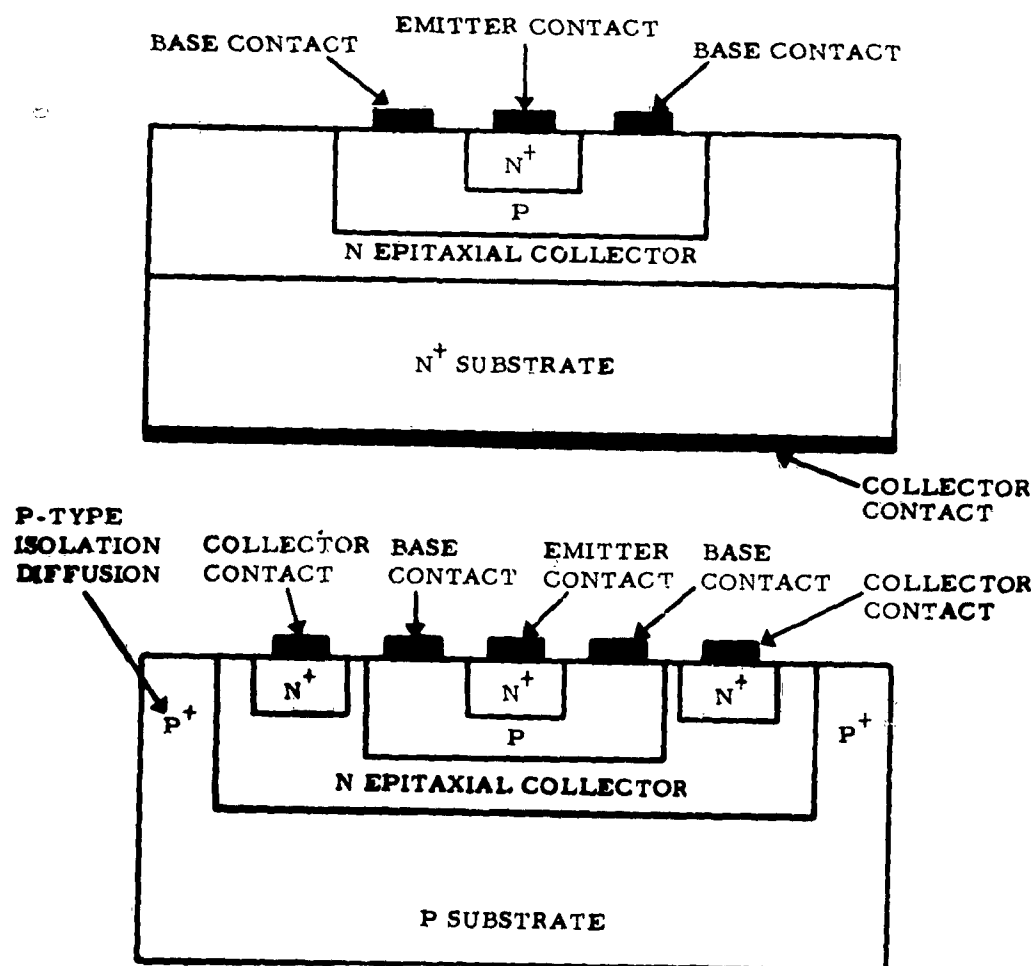


Figure 2-2. Comparison of Cross Sections of Integrated Transistor vs Discrete Transistor

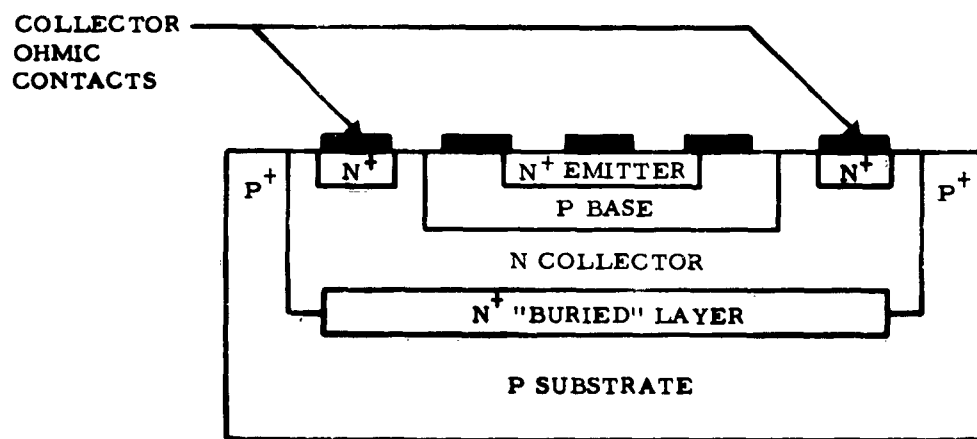


Figure 2-3. Utilization of "Buried" n^+ Layer to Reduce Collector Series Resistance

TABLE II-1
DTL CIRCUIT PERFORMANCE COMPARISON TABLE

Integrated Circuit Parameter	Hybrid or Discrete Circuit	Monolithic Circuit (0.1 ohm cm-25 μ epi.)	Buried-Layer Monolithic Circuit (0.5 ohm cm-12 μ epi.)
Total parasitic capacitance:			
Input node, pF	—	13.95	6.70
Output node, pF	—	6.52	3.12
Input characteristics:			
Forward current, mA	5.8	5.7	5.8
Reverse current, μ A	0.01	0.01	0.01
Output characteristics:			
ON voltage at 35 mA	0.24	0.34	0.25
OFF voltage	3.0	3.0	3.0
Switching speed ($C_L = 20$ pF):			
Turn-on time ($R_L =$ 100 ohms), ns	16	26	20
Turn-off time, ns	26	38	34
Propagation delay time, ns	10	16	13

4. Resistors

In addition to the transistor and diode, the fabrication of resistors and capacitors has been achieved in the bulk silicon thus forming complete logic circuits in the chip. In silicon, resistors are formed by the diffusion of p-type base region into an isolated n-type collector region. An aluminum metalization is used to provide the required ohmic contacts. The resistance value is given by:

$$R = R_{BB} [L + K] \text{ ohms}$$

where

R_{BB} = sheet resistance of the p-type diffusion, ohms per square

L = resistor length, and

K = correction for end contacts.

Sheet resistance is inversely proportional to resistor width. For a resistor one-mil wide, R_{BB} is of the order of 200-ohms per square. High ohmic values achieved through narrow widths are precluded by yield limitations. Current technology achieves resistors of 20 percent tolerance for one-mil width and 10 percent for two-mils. Temperature coefficients are on the order of 0.1 percent or three times their discrete counterparts. A general rule of thumb: if the circuitry desired requires more than 1/2 the die area for resistance (or capacitance), the use of standard monolithic integrated circuitry is questionable.

5. Diodes

Monolithic diodes are formed by an emitter base junction or a collector base junction. The former offers two choices: the collector can be shorted or open-circuited. This is accomplished by aluminum metalization. Choice of the proper configuration requires detailed consideration of the effects of parasitic capacitance vs. leakage currents on the logic switching speed. Equivalent circuits of the three diode types are shown in Figure 2-4. In each case, the existence of a parasitic transistor is seen from whence originates a leakage current problem. The use of gold diffusion in the silicon bulk significantly reduces minority carrier storage time, resulting in parasitic transistor current transfer ratios of the order of 0.001 or less.

6. Capacitors

The monolithic capacitor is equivalent to the conventional parallel plate variety. Figure 2-5 illustrates the monolithic capacitance cross-section. Silicon dioxide, a dielectric, is sandwiched between one metal plate fabricated during the aluminum metalization, and another consisting of an n^+ region formed during emitter diffusion. Monolithic capacitors are independent of voltage. Their principal disadvantage is the large area requirements. (This is true also of the thin-film fabricated types.) At a dielectric thickness of 500 Å, the capacitance per unit area is only 0.35 pF/mil². Figure 2-6 illustrates the equivalent circuit.

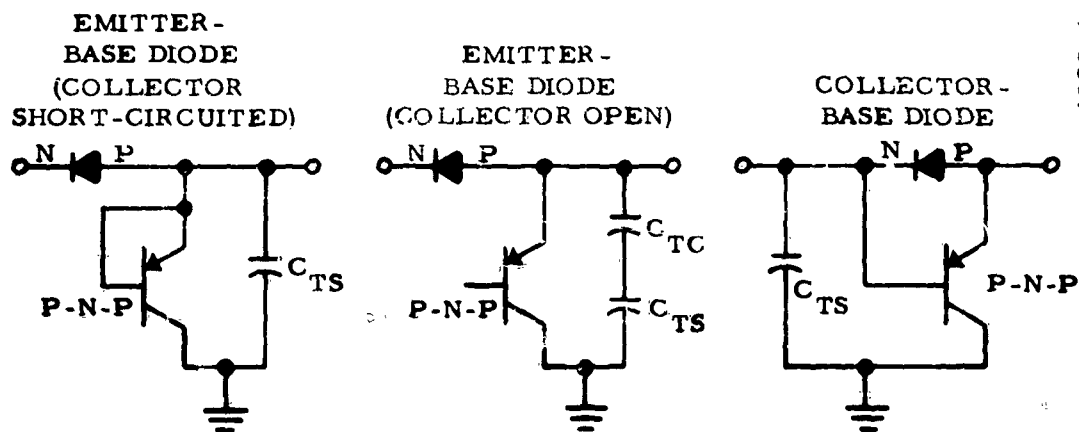


Figure 2-4. Equivalent Circuit and Minority-Carrier Storage Diagrams

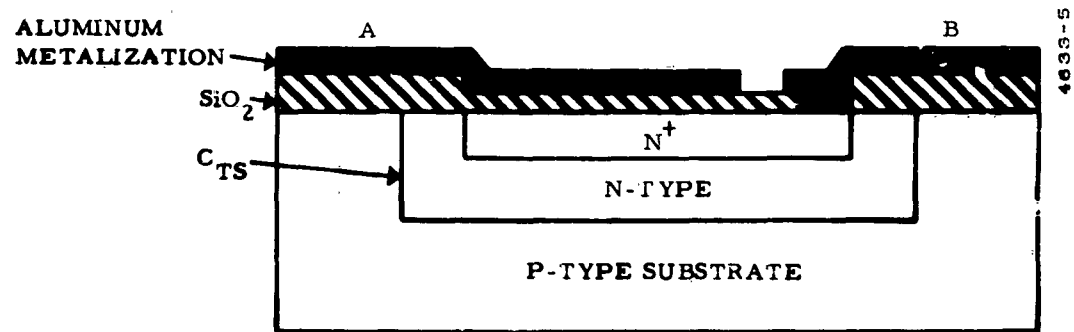


Figure 2-5. Cross Section of an Oxide-Type Capacitor

$C = 0.35 \text{ pF/mil}^2$ AT 500 Å OXIDE THICKNESS

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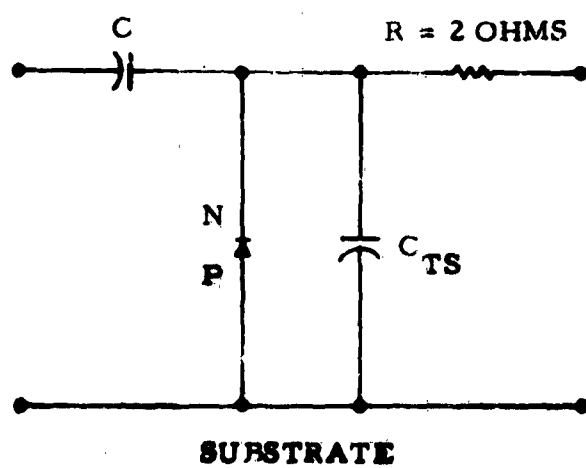


Figure 2-6. Equivalent Circuit of an Oxide Capacitor

7. Diffusion Processes

Discrete planar epitaxial transistors are manufactured with two **diffusions**. Monolithic silicon circuits require four diffusions, and hence are called double-diffused. These are:

- a. Antimony or arsenic (n-type) diffusion prior to epitaxial deposition — performed immediately below base of transistor, to obtain the lowest RC time constants possible.
- b. Isolation Diffusion — a boron (p-type) diffusion through the epitaxial layer to link with the substrate. The reverse biased p-n junctions, so formed, serve as isolation elements between all circuit components.
- c. Base Diffusion — This diffusion forms the basis of all transistors and, usually, the resistors. This is a boron (p-type) diffusion.
- d. Emitter Diffusion — A phosphorous (n-type) diffusion with maximum dopant concentration used to form the emitter and cathodic terminal of monolithic diodes.

In all, seven masking operations may be required. Four are required for the above diffusions. The remaining are required to produce the contact windows for metalization, the aluminum metalization, and capacitors if used by the circuit.

8. Logic Forms

A wide variety of logic circuits has been made available through the use of monolithic circuit technology. DTL (diode — transistor logic), DCTL (direct coupled transistor logic), RTL (resistor coupled transistor logic), TTL (transistor coupled transistor logic), CML (current mode logic), and variations thereof have been marketed widely. Additionally, flip flops are also available for counting and register applications. The individual gates, or in some instances, double gates are diced from a master wafer. This master slice of about one inch in diameter may contain up to 1200 transistors/diodes from which may be formed up to 400 logic gates. DTL, DCTL, RTL, TTL, and CML have been available dating from the period when discrete components (passive and active) were used exclusively. During this early period, DTL enjoyed the highest popularity due to its superior performance and cost factors.

However, the batch fabrication of the entire logic circuit in the bulk silicon requires a reappraisal of the relative merits of the above logic circuits. Parasitic, tolerance considerations, and adaptability to micro-electronic packaging are especially to be considered. Other important aspects include the number of isolation regions required, total resistive and capacitive area requirements, and economics of transistors vs. diodes and passive components.

9. Parasitics

Figure 2-7 shows the various capacitances inherent in an integrated logic circuit. These result from the interfaces between the various semiconductor layers and the capacitances formed by the SiO_2 dielectric between the metalization layer and the P-Type substrate. Typical values of the capacitance (per square mil of junction area at zero volts bias) are: $C_1 = 0.02$ pf; $C_2 = 0.1$ pf; $C_3 = 1.1$ pf, $C_4 = 0.01$ pf.

The cross-section of various diode structures, previously discussed, are shown in Figure 2-8 and the equivalent circuit showing parasitic transistor action in Figure 2-9. The parasitic transistor action results from the four-layer transistor inherently contained within the diode configuration. Selection of the diode configuration most appropriate to the circuit requirement minimizes the parasitic transistor action.

A further consideration relative to parasitics in integrated circuits concerns isolation regions. These regions are required to achieve isolation, on site, of the component groups contained within the single crystal of silicon. Figure 2-10 illustrates the requirements for isolation regions in a typical DTL circuit. The capacitance associated with a 6×8 mil isolation region for a substrate resistivity of 0.1 ohm-cm and one mil epitaxial thickness is:

$$C_{TS} = C_{TS(\text{bottom})} + C_{TS(\text{sidewall})}$$

$$C_{TS} = \frac{0.08 \text{ pf/mil}^2 (6 \text{ mil} \times 8 \text{ mil})}{V} + \frac{0.17 \text{ pf/mil}^2 (28 \text{ mil} \times 1 \text{ mil})}{3 V}$$

where V is the reverse voltage applied from collector to substrate. For a value of $V = 5$ volts, $C_{TS} = 4.46$ pf.

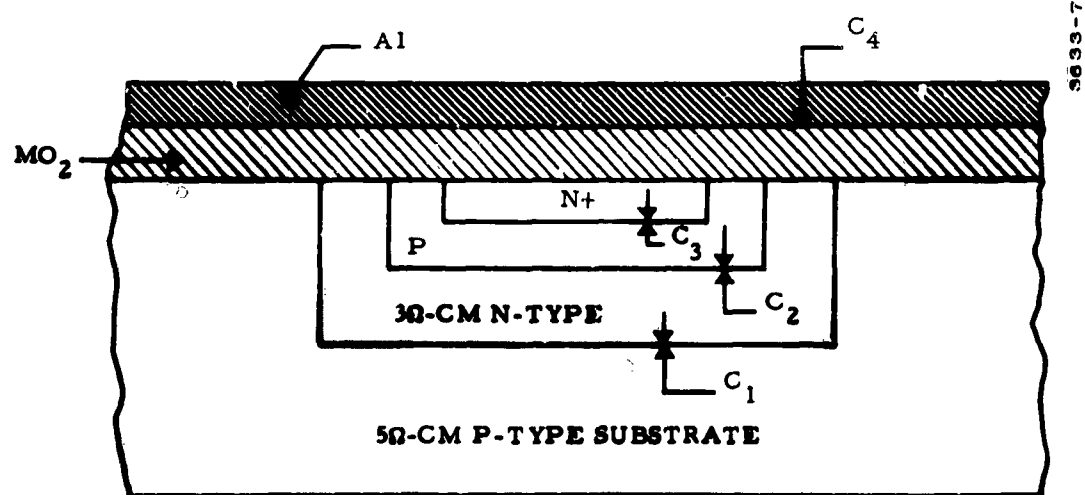


Figure 2-7. Capacitance Associated With Junction of Typical Circuit

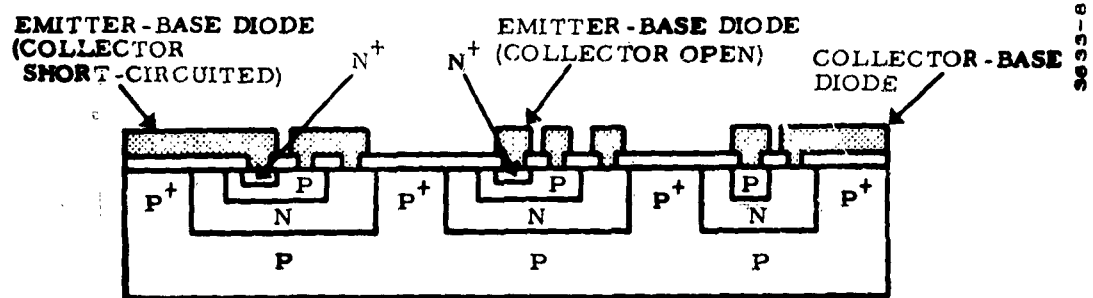


Figure 2-8. Cross Section of Various Diode Structures

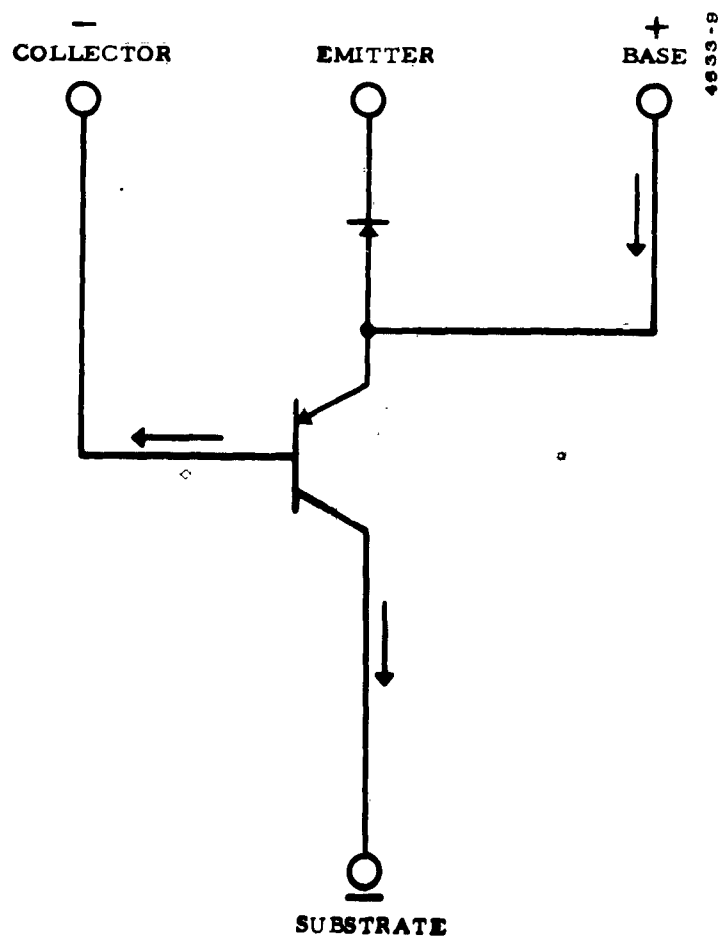


Figure 2-9. Equivalent Circuit of Four-Layer Transistor

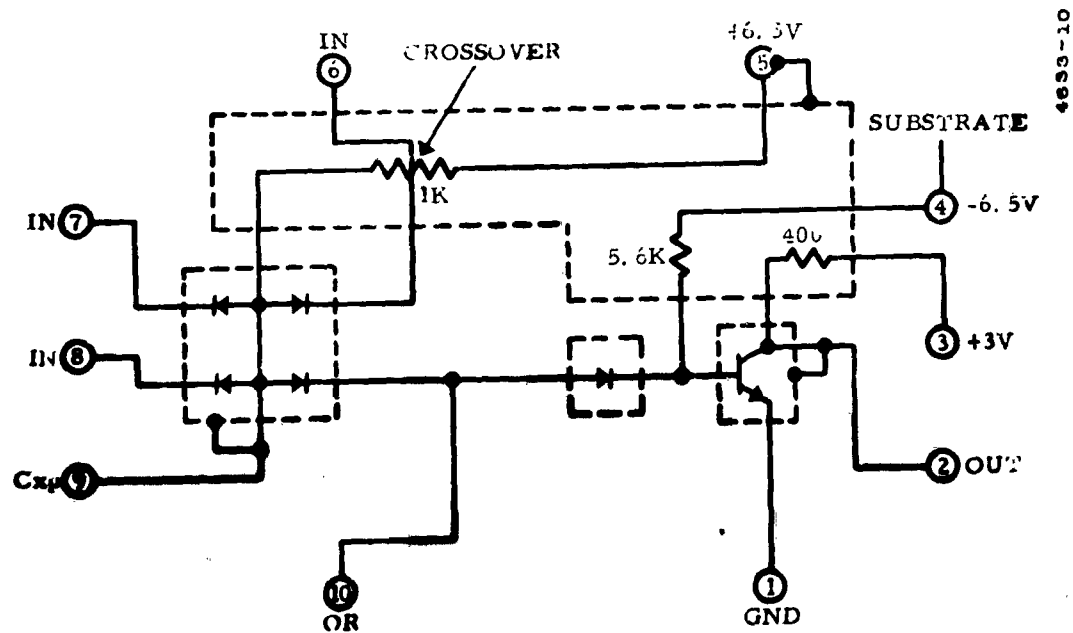


Figure 2-10. Schematic Diagram of DTL NAND Gate Showing Isolated Regions

Observations relative to isolation regions are as follows:

- a. They represent non-productive area on the chip, and
- b. They reduce speed through added parasitics.

Logic forms minimizing the number of isolation areas are to be preferred. Use of higher collector resistivity (0.5 ohm-cm) reduces the capacitance by one-half. However, as was previously discussed, this would undesirably increase the collector saturation voltage. The use of buried layers to form a low resistance shunt between the collector and substrate interface obviates this difficulty.

10. Tolerances

The more severe tolerance problems in monolithic integrated circuits result from the inherently larger tolerance spreads associated with monolithic passive components. Tolerances of monolithic resistors and capacitors are 20 percent typically. However, ratios of resistors can be held to an accuracy of 2 percent or better. Temperature coefficients are on the order of 0.1 percent.

Monolithic transistors have performance equivalent to discrete types with the exception of a slight penalty in f_{max} (highest frequency at which the transistor can be made to oscillate). This performance is attributable to improvements in epitaxy, masking, and isolation resulting in current gain (β), saturation voltage (V_{GSAT}), and leakage current (I_{CBO}) of the same magnitude as discrete transistors. Further improvements may be expected, principally in masking accuracy, with the result that ultimate bandwidth up to 60 gc will be feasible.

11. Adaptability to Micro-Electric Packaging

Logic forms which minimize the area of the silicon die required per gate, and the power for a given speed facilitate micro-electronic packaging. This provides further motivation for minimizing passive components (inefficient on an area basis) and isolation areas (waste area plus additional parasitics).

The optimum number of gates that can be packaged together is related to the mode of signal transmission and the number of leads available in the package. Serial transmission is far more conservative of input/output terminal requirements as compared to parallel transmission.

Computer organizations using serial transmission without the penalty of speed sacrifice have an obvious advantage.

The number of leads available is a function of the package shape and size. This is an area where much progress is required. Current state-of-the-art includes flat packs, round packs, modified TO-5, etc. with 12 to 20 leads. This is sufficient to handle the range from 2 to 4 gates which are independent. However, major terminal savings result when the gates are functionally related in such configurations as full-bit shift register, counter, or adders.

Characteristics of the idealized component package have been postulated by Rice⁴. These are:

- a. In-line terminals in one side for
 - (1) Best intraconnection efficiency
 - (2) Easy design layout
 - (3) Easy lead straightening
- b. Short rigid-pin terminals for
 - (1) Easy insertion
 - (2) Relaxed drilling tolerances
 - (3) Allowing rougher handling
 - (4) Eliminating special handling fixtures
 - (5) Allowing flow or wave soldering
 - (6) Easy replacement in field
- c. Linear package mounted perpendicular for
 - (1) Best configuration for forced air cooling
 - (2) Easy conversion to high density system
- d. A single monolithic die with largest circuit function(s) economically obtainable and broadly useful to
 - (1) Circuits can be defined by logicians, circuit and device engineers
 - (2) Throwaway items are smaller and less expensive

- (3) Stocking problem is less complex
- (4) Manufacturing yields can be maximized
- e. 0.075-inch pin spacing
 - (1) For low cost systems where density is not critical
 - (2) To match easy drilling tolerances in printed-circuit boards
- f. 0.05-inch pin spacing
 - (1) For systems where density is more important than minimum costs

12. Power

The requirements of avionics computers in terms of speed, noise margin, and logic interconnectability dictate logic gate power levels in the 1-10 milliwatt range. Thus, arrays of 100 gates (which is beyond the current state-of-the-art for bipolar transistors) would dissipate from 0.1 to 1 watts. Such levels present no cooling difficulties with compatible package sizes, say 0.3 X 0.3 inches for the 100 gate array.

13. Performance Factors

The factors to be evaluated and traded off relative to performance are speed, fan out, noise margin, and power. While these could be expressed in a single figure of merit, for example

$$\frac{(\text{Speed}) \times (\text{Fan Out}) \times (\text{Noise Margin})}{\text{Power}}$$

there is little point in doing so. The reason is that these parameters are not independent variables. However, the speed/power ratio does have merit and can be plotted with fan out as a parameter. Equations for this ratio can be developed for use in design optimization.

14. Speed

The speed (switching time) of transistors used as binary gates is essentially determined by the time required for the base current to supply charges to or remove charges from the capacitive elements in the transistor and circuit. Storage time, a saturation phenomenon, has

become insignificant due to such processes as gold doping reducing minority carrier life times. The implications to integrated switching circuits are two fold:

- a. Saturated logic will have a very slight penalty over non-saturated logic and therefore is to be preferred.
- b. Integrated circuits will be somewhat slower than discrete types due to higher parasitic capacitance.

The equation for rise time and fall time contains the factor⁵

$$\frac{1}{\omega_T} + R_L \bar{C}_c$$

where ω_T is the large-signal average gain-bandwidth product, R_L is the transistor load, and \bar{C}_c the large-signal average collector capacitance. Thus, both rise and fall times are decreased by greater ω_T (implies higher masking accuracies) and higher power.

The equation for rise time is also a function of the base current, I_{B1} . Thus, low input resistance in the base is also important to minimize rise time.

15. Fan-out and Fan-in

Fan-out specifies the numbers of loads driven by a logic gate while fan-in specifies the number of inputs into the gate. Fan-out and fan-in are important from a logic design standpoint because these quantities specify the number of logical levels required, hence, the delay in achieving the give logic function. Fan-in also exerts strong influence on the number of terminals required and packaging format. Previous tabulation of fan-in and fan-out in computers shows the highest usage to be three, but a broad range up to 15 is frequently required. A satisfactory compromise in terms of logic delay, number of terminals, and number of packages has been to design a fan-in and fan-out from 5 to 8.

Fan-in and fan-out also can be shown to relate to speed and power. In general, the (fan-in) x (fan-out) product has an optimum with respect

to the speed/power ratio. Large (fan-in) x (fan-out) products are disadvantageous with respect to this ratio, which provides additional motivation to avoid a design with the capability of accepting the worst case required purely by Boolean logic considerations.

16. Noise Margin

The relationship between the input level and the output level in the inverting gate is specified by the transfer characteristic, see Figure 2-11. Input levels of excitation can be defined with respect to the transfer characteristic which cause the gate to change state. For an input level less than or equal to MAX ZERO, the output level will be greater than or equal to MIN ONE. When the input level is greater than or equal to MIN ONE, the output level will be less than or equal to MAX ZERO⁶.

For the gate to change state, the input level must change from below MAX ZERO to above MIN ONE if in the ONE state and vice versa if in the ZERO state. As can be seen, the greater the voltage difference between the quiescent levels (ONE and ZERO) to the transition levels (MIN ONE and MAX ZERO), the greater the noise margin. Thus, noise margin improves with greater signal swing, or equivalently, higher power.

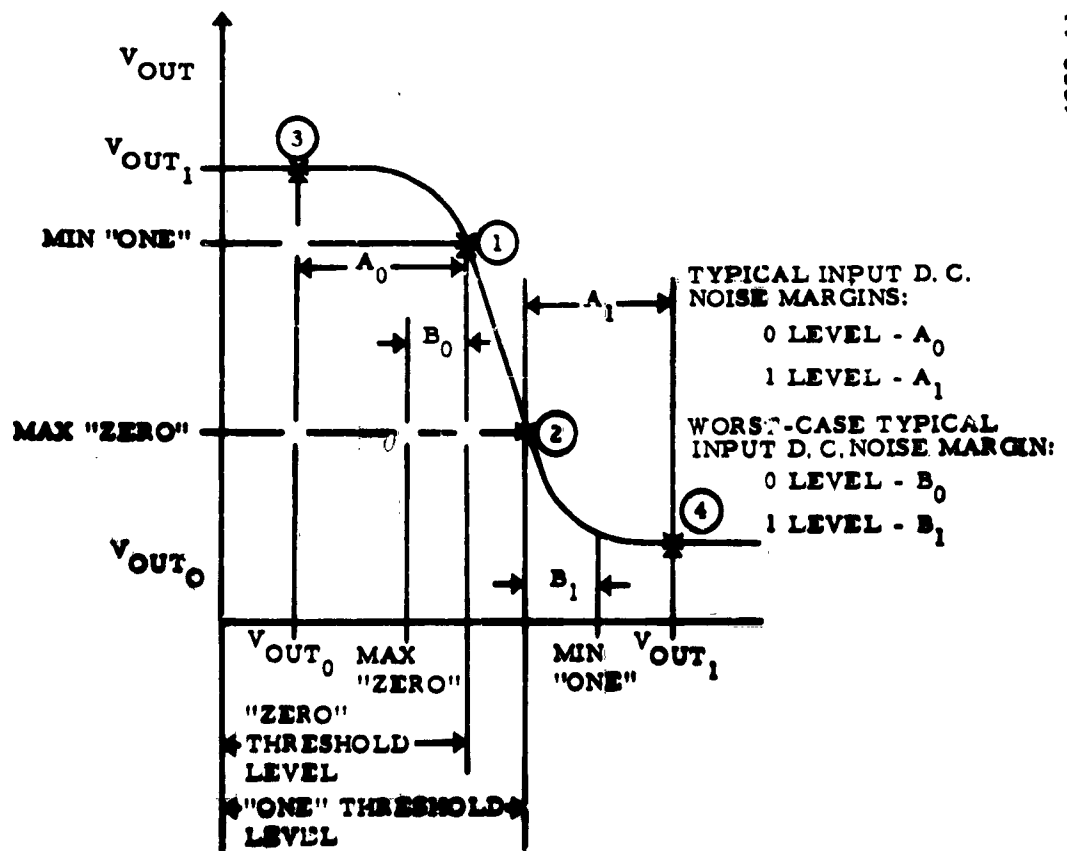
17. Power

From the preceeding discussions, it is apparent that the performance factors of speed, fan-out, and noise margin are all tradeoffs with power. Improvements in each of these are accompanied by higher power levels. Higher speed imply lower $R_L C_L$ products. Fan-out is approximately proportional to current gain. Noise margins are improved by higher signal swings.

A power level consistent with system requirements for these factors is required. As indicated previously, this falls in the range of 1-10 milliwatts per gate. A dissipation factor of 1-10 watts per square inch is compatible with conventional packaging techniques, thus indicating true feasibility of arrays of 1000 gates.

18. Comparison of Logic Circuit Types

Performance factors desirable for integrated logic circuitry include: Intermediate speed (1-5 mc/s); power efficiency (1-10 milliwatts/gate);



4000-11

Figure 3-11. Input-Output Transfer Characteristic

fan-out, and adequate noise margin. The logic circuits in current usage have all been inherited from their discrete counterparts. Figures 2-12 and 2-13 shows each type. Also refer to Table II-2.

TABLE II-2
COMPARISON OF LOGIC CIRCUITS

Circuit Type	Propagation Speed	Power	Noise Immunity	Fan-In x Fan-Out	Gate Area*
RTL	5	4	4	5	5
DTL	3	2	1	2	3
DCTL	2	1	2	3	2
TTL	2	1	3	1	1
ECTL	1	4	5	3	4

NOTE: 1 is the highest rating

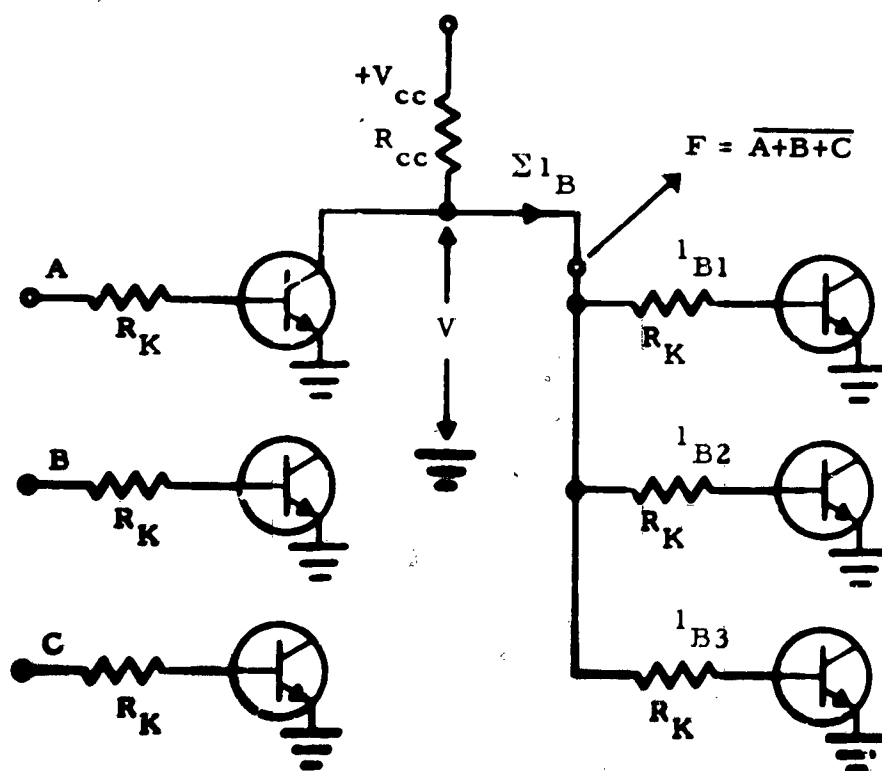
*This factor is made proportional to the sum of

- a. the number of components (fan-in of 5)
- b. the number of isolation regions
- c. the total circuit resistance in KIL ohms

19. RTL

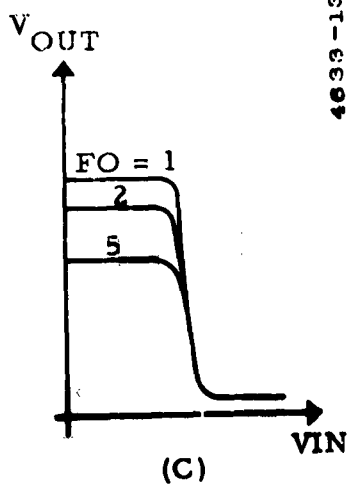
RTL logic achieves isolation between gates by employing large coupling resistors. In batch technology, diffused resistors possess no cost advantage over active devices. Where reasonable tolerances are required, their costs and space utilization on the chip are decidedly inferior to diodes. The larger ensuing RC constants limit device switching speeds. For these reasons, RTL is not advantageous in batch technology.

(In hybrid thin-film technology, fabrication of resistors of 3 percent tolerance and low temperature coefficients is routine. Thus, where maximum logic speed is not required, RTL has potential application to this case.)



4693-12

Figure 2-12. The DCTL Circuit



4633-13

Figure 2-13. The Effect of Fan-Out Loading on the Voltage-Transfer Characteristic

20. DTL

DTL retains its excellent performance (noise margin, fan-out, power, speed) in batch circuits, though the economic advantage over TTL is no longer true. The coupling diodes isolate source and input, with the result that distribution of output current is not a problem.

Circuit performance is a function of the monolithic diode configuration and geometry chosen (see previous discussion). The configuration employing a common base region (collector open) corresponds to the TTL logic form and will be commented on below. The case for separate vs. common base regions (collector shorted) is a trade-off of diode recovery time vs. space requirements. The collector base-diode configuration with isolated collectors has low leakage and improved speed. The speed improvement results from lower effective time constants due to the fact that the parasitic substrate capacity is driven from a lower source impedance.

Fan-out in DTL circuits is limited by the current absorbing capability of the transistor in the ON state. With respect to noise margin, insertion of a diode in coupling network increases the noise margin by the diode breakdown voltage.

21. DCTL

Without the base input resistors, unsatisfactory operation is realized due to the tolerance spread of the base input characteristics. The result is current "robbing" by the transistor with minimum dynamic input impedance. The base input resistors must be kept low if speed of the order of 1 mc/s is required. Low transistor storage time is required to avoid turn off delay due to hard saturation.

Fan-out in DCTL circuits is limited by the increase in leakage current through the load due to paralleling of collectors. This decreases the output during the "off" state as shown by Figure 2-13.

22. TTL

In TTL, coupling is provided by a multi-emitter transistor. Because the coupling transistor is always on, TTL has high speed of operation. Power dissipation is low because of low signal swing. A common supply may be used for the switch and coupling transistor. These factors all favor TTL for batch technology.

23. Other Logic Forms

The above logic types have seen widest application in avionic computers. They are all forms of saturating logic - wherein the device is operated into saturation in its "turn-on" state.

Two forms of non-saturated logic are CML - current mode logic, and ECTL - emitter coupled transistor logic (a modified CML). While these offer the highest speed, they also are the most inefficient from a power dissipation standpoint. The reduction in voltage separation between 1 and 0 states, due to non-saturation, also indicates higher susceptibility to noise. Further disadvantages from a batch fabrication standpoint include a minimum of two supplies required and higher usage of resistor components.

24. Cost of Monolithic Integrated Circuits

The mass production techniques employed for monolithic circuits will result in significant cost reduction, as illustrated by the following example: Consider a wafer 50 x 50 mils. Such a wafer can contain up to 500 individual circuits. The cost to carry the wafer through the required diffusion and metalization steps is approximately \$10.00, including normal overhead. Assuming 100 percent yield, the cost per individual circuit is 2-cents apiece. Even with a yield as low as 50 percent, the cost a complete monolithic circuit is only 4 cents. In comparison, the unconnected components for a discrete logic circuit circa 1960 ran in excess of \$2.00 in high volume production.

Thin-Film Circuits

Present thin-film circuits are hybrids as contrasted to "Monolithic" integrated circuits. That is, thin metallic films provide the passive components with the active components supplied by conventional type discrete components. The films employed are generally less than 5000 Å (10^8 Å = 1 cm), hence the qualification thin. Materials which have been used for the films include tantalum, titanium, niobium, and cermet. Active devices employed with thin films are generally in the form of glass-coated silicon chips, although standard TO-5 transistor and DO-18 microdiode packaging has also been used. Requirements for the glass coating include low water absorption and low component leaching which are met by several available glasses.

The most extensive film technology available for passive components are the tantalum* and the cermet** methods. Tantalum provides resistors, capacitors, as well as rudimentary interconnections. In contrast, the cermet technique is not based on a single metal but employs chromium, nichrome, or silver-palladium films for resistors; and silicon monoxide, titanium oxide, etc. films for capacitors. The all tantalum technology simplifies materials processes whereas the cermet provides a greater range of resistance values.

1. Substrates

The films, whether tantalum or cermet, are deposited on glass, mylar, or glazed alumina ceramic substrates. Films substrates must be suitable with respect to smoothness of surface, chemical composition, and thermal conductivity.

Surface smoothness is required on the order of 1 micro-inch. Both glass and glazed ceramic substrates produced in drawn sheets meet this requirement. Polishing techniques are avoided due to the propensity for embedment of foreign materials.

Chemical composition is critical with respect to alkali metal content. Sodium ions, wandering into tantalum-nitride resistors, cause changes up to 10 percent in resistance value. Thus, glass substrates of low alkali content are imperative. Glazed alumina is immune to this problem.

With respect to thermal conductivity, the alumina substrate offers important advantages. Tantalum-nitride resistors exhibited little temperature aging on the alumina at power levels up to 1 watt, whereas on glass, 10-15 per cent changes can be expected. This result is due to alumina ceramics exhibiting thermal conductivity in the neighborhood of 12 BTU/hr/°F which is about the figure for stainless steel.

Thus, with respect to substrates, glazed alumina is superior to glass. However, for low power applications, glass is often favored because of its low cost and ease of cutting to required size from large stock.

*Developed by Bell Telephone Laboratories

**Now in commercial use by International Business Machines

2. Processes

The three most prominent plating methods for films are sputtering, evaporation, and anodization. Sputtering is the process of ejecting the atoms to be plated from the source by bombarding it with inert gas positive ions. Sputtering has become the preferred deposition technique because of its applicability to a large number of substances. It provides superior uniformity of deposition over wide areas. In addition, in the deposition of alloys, sputtering maintains constant composition throughout the run. Evaporation is used for metal and cermet resistor types, magnetic films, and some inorganics. Its advantages include simplicity of apparatus, high film purity, reasonable deposition uniformity, and minimum deposition time. Disadvantages include narrow angle of incidence limitations and decomposition of some compounds when subjected to evaporation temperatures.

Anodization is chiefly used for the formation of insulating oxide film required for resistors and capacitors in tantalum film technology. Thickness control is of good quality.

3. Circuit Fabrication

The sequence of steps in the fabrication of a typical tantalum hybrid thin-film circuit are as follows:

- a. Sputtering of tantalum over entire substrate.
- b. Application of photo resist to substrate.
- c. Exposing substrate, through desired film mask.
- d. Developing and selective etching of the interconnecting conductor and resistor patterns.
- e. Electrolytic anodization or abrasion to trim resistors and passivate them.
- f. Joining chips to substrate.

Circuits with a component tolerance of 10 per cent can be produced through automated non-adjusted methods at high yield using tantalum films.

Where tolerances as low as 3 percent are required, anodizing of the resistors with feedback monitoring of the resistor value is used. Precision of as high as .05 percent have been attained where monitoring equipment of suitable precision was applied. A further advantage of tantalum film resistors is their negligible parasitic capacitance, making them ideal for analog-digital conversion networks, parallel T structures, etc.

4. Packaging

The substrate is the primary level of packaging. Connections to the interconnecting land pattern are made through pins inserted in holes in the substrate. One form factor that has been wide commercial application is 0.27" x 0.27" x .04" containing an average of 6 transistors and 2 resistors.

Comparison

Hybrid thin-film circuits form the basis of an extensive line of commercial and military computers. A high degree of automated fabrication of films has been achieved as exemplified by the Naval Avionics Facility at Indianapolis and the Western Electric Thin-Film Continuous Vacuum Processing Machine. These have established the films as low cost technology, especially where large production runs are required. Other advantages claimed include:

- Optimum circuit design due to wide selection of active devices.
- Wider range of resistance values with lower tolerances and temperature coefficients.
- Higher frequency operation due to electrical isolation of components as well as tight packaging.

Monolithics, however, are now challenging both the cost aspects and performance aspects. As previously indicated, performance of monolithics approaches that of the discrete facricated circuit. The employment of a single automated technology for the entire digital circuit will be almost impossible to beat from a cost standpoint. Preliminary evidence also suggests higher reliability for the monolithics due to the drastic reduction in soldered contacts required. Finally, there is a minimum of a 3/1 advantage in packaging density over thin-film hybrids.

Current status of film and monolithic technologies for passive components is shown in Table II-3⁷. With the achievement of more ideal isolation, the odds are that monolithics will monopolize the post 1970 computer field.

Future State of the Art

Three technologies are being pursued in an attempt to achieve the advantages of batch fabrication of digital circuit arrays comprised of up to 1000 active devices on a wafer:

- Thin Films - active and passive
- MOS (Metal-Oxide-Silicon)
- Monolithic, bipolar, silicon

Thin-film fabrication of electronic circuits has been intensively pursued for more than five years. Progress in passive circuit deposition has already been discussed; the active thin-film device, however, has proven a most elusive goal, this despite numerous attempts. Latest attempts in this field are concerned with the deposition of silicon films on sapphire substrates. One of the difficulties has been the inability to consistently achieve single-crystal films, without which device performance, reliability, and producibility must remain inferior to monolithic transistors. It may be stated, categorically, that no known realization of active thin-film device approaches that of conventional bulk produced transistors. Thus, in this analysis of the future state of the art, attention will be concentrated on two developments exploiting bulk silicon properties: **MOS and monolithic bipolar silicon arrays.**

MOS

1. Introduction

The most advanced of the batch fabrication* technologies is the MOS field effect transistor. MOS is an abbreviation for metal-oxide-semiconductor, the three layers of material of which the device is

*Batch fabrication - The simultaneous manufacture of a multiplicity of identical devices and their subsequent application without necessity for individual separation.

TABLE II-3
COMPARISON OF PASSIVE COMPONENT CHARACTERISTICS

Resistors	Sheet Resist. Ohms/SqLare	Temp. Coeff. ppm/°C	Tolerance without trim %	Tolerance with trim %	Drift at T /1060 h
Si (diffused, R type)	100 - 300	1000	7 to 20	N. A.	small
Si (diffused, N type)	up to 10	800	5 to 20	N. A.	small
PdAg Cermet (screened)	1 - 100 K	$\leq \pm 250$	10 to 20	± 1	$< 1\%/150^\circ\text{C}$
Nichrome film	up to 300	± 200	5 to 10	-	$< 2\%/100^\circ\text{C}$
Chromium film	20 to 800	up to 2000	-	-	$1\%/80^\circ\text{C}$
Sputtered tantalum film	up to 100	± 150	5 to 10	± 1	$1\%/125^\circ\text{C}$
Tantalum nitride film	5 to 75	up to -00	-	± 0.1	$< 0.1\%/25^\circ\text{C}$
Cr-SiO cermet film	10 to 20 K	± 75	5 to 10	± 1	$< 0.2\%/125^\circ\text{C}$

Capacitors	$\mu\text{F V/cm}^2$	Temp. Coeff. ppm/°C	Practical limit pf/mil ²	Practical Q at f	Tolerance
Si PN junction	-	100	0.018 to 0.2	-	10 - 20
Screened, titanate filler	7	300 and up	0.1 (450 V)	50 at 1 mc	15
Screened, TiO ₂ filler	< 1	-	0.01 (450 V)	> 50 at 1 mc	15
SiO	< 1	-	.03 (40 V)	24/70 mc	15
Ta ₂ O ₅ on Ta	5.5	250 - 1000	4 (8 V)	2.5/5 mc 200/1 kc	5 - 10
Ta ₂ O ₅ on Ta and Al	5.5	250 - 1000	4 (8 V)	25/5 mc	5 - 10

Inductors	Outside diam. inch	Numbers of turns	Inductance micro-henry	Q	Film Thick- ness Microns
Vacuum deposited Cu	0.429	18	2.1/70 mc	13/70 mc	1.2
Cu re-inforced by plating	0.167	4.5	0.1/70 mc	26/70 mc	12

By R. Thun, "Potential and Limitations of Thin-Film Circuits"

comprised. In contrast to the bipolar junction transistor which uses minority injection and survival phenomena, the MOS operates with majority carriers.

As late as 1963, few companies were conducting research and development in MOS. Today, thirteen companies are active in MOS and nine of these market one or more MOS devices. Considerable success has been achieved with device fabrication. At least two companies are offering complex arrays of MOS devices. Others, more heavily committed to bipolar technology production, are undoubtedly as far advanced in a technical sense. However, due to current heavy commitments, their present planning is for one-half year to one year delay before actively marketing MOS.

The current technology has largely an empirical basis. Key processes are closely guarded trade secrets. Such is the complexity of the three phase material system of the MOS that a satisfactory quantitative theory of its physics and chemistry is still unavailable. Until such a foundation has been constructed, the ultimate from this technology will not have been achieved.

Primary application of MOS is to switching and multiplexing. These applications are of fundamental importance to avionics systems, not only in the central computer complex, but also in peripheral processing areas concerned with navigation, automatic flight control display, etc. Briefly, the weight, size, power, reliability, and cost parameters appear to afford the highest degree of functional automation in the entire avionics system as may be desirable from effectiveness considerations.

Figure 2-14 shows the MOS geometry. Pertinent features are the N-doped silicon body into which are diffused two p-type regions spaced L-units apart and W-units wide; an insulating layer of silicon dioxide covering the entire structure with the exception of two metalization areas; and three electrodes providing the gate, source, and drain. When sufficiently negative voltage is applied to the gate, conduction occurs between the drain and source regions. Physically this is explained by the formation of an inversion layer at the surface of the semiconductor between the two p-type regions. In the inversion layer channel, the hole concentration is dominant owing to the repulsion of electrons and attraction of holes by the negative gate voltage.

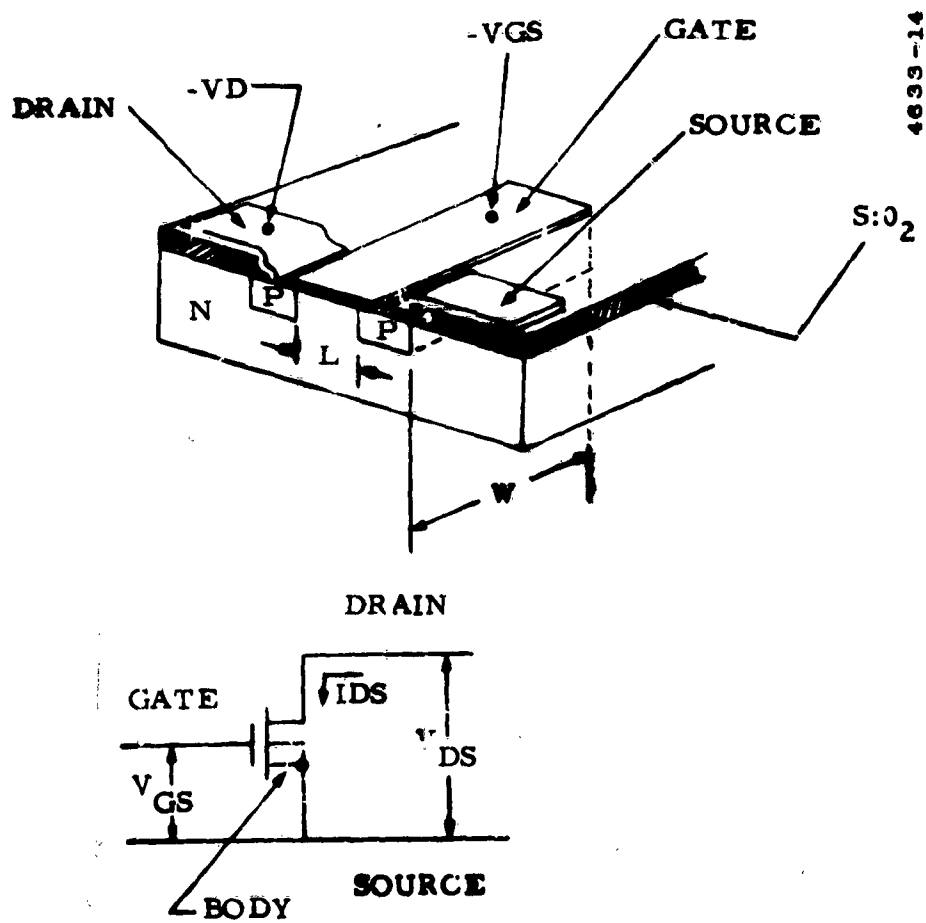


Figure 2-14. MOS Geometry and Symbol

2. Operation of MOS FET

The operation and principles of the MOS have been well documented in the literature. Therefore, this review of MOS operation will be brief. The interested reader may refer to the literature for more detailed information.

The MOS FET may be operated in two modes: the depletion mode and the enhancement mode. In the depletion mode, shown in Figure 2-15, the MOS is normally "on" due to the built-in channel. As the gate voltage is increased, the channel is depleted or made more narrow, reducing the drain-source conduction. Further increase in the gate voltage causes the depletion regions to come in contact with one another, at which point conduction ceases. This is the so-called "pinch-off" point. The lack of a sharp threshold in the depletion mode precludes its use for digital integrated circuits.

The enhancement mode MOS does not have a built-in channel (see Figure 2-14). In this mode, both the drain and the gate are operated with the same voltage polarity, thereby requiring only one supply for MOS logic. As previously indicated, the polarity required for the enhancement mode back-biases the device, resulting in self isolation. No conduction occurs until the gate voltage exceeds a threshold on the order of 5 volts.

These characteristics are very useful for digital integrated circuit applications. The quantitative relations for switching may be stated in terms of the threshold voltage for conduction and the relation between the source to drain current, the control (gate) voltage, and the physical parameters of the device.

The threshold voltage is given by the following equation:

$$V_T = \frac{-(Q_{ss} + Q_B) X_o}{K_o C_o}$$

Where Q_{ss} is the surface state charge, Q_B is the bulk charge, X_o is the oxide thickness (equal to 0.15μ for $V_T \approx 5$), K_o is the relative dielectric constant of the oxide, and E_o is the permittivity of free space (8.85×10^{-14}) farad/cm. Increase in the gate voltage beyond the threshold point increases the current according to the following equation

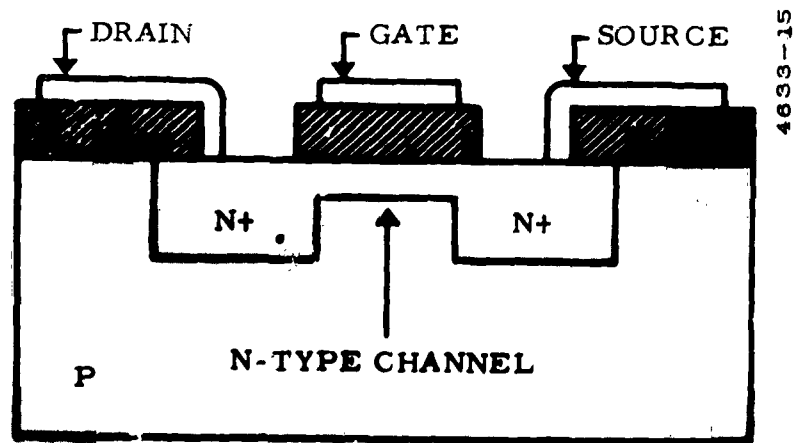


Figure 2-15. Depletion Mode MOS

$$I_{DS} = \frac{\mu_p C_o}{2L^2} (V_G - V_T)^2 \quad (2)$$

where I_{DS} = saturation source to drain current

μ_p = effective mobility of holes in the channel
(about 1/2 the bulk mobility)

C_o = capacitance of the oxide layer under the gate electrode

L = channel length

V_G = gate voltage

The gate capacity, C_o , for width is given by

$$C_o = \frac{K_o e_o WL}{X_o} \quad (3)$$

Combining this result with (2)

$$I_{DS} = \frac{\mu_p K_o e_o W}{2X_o L} (V_G - V_T)^2 = \frac{W}{L} (K) (V_G - 5)^2 \quad (4)$$

Equation (4) confirms the previous qualitative discussions. The square law increase in conductance requires larger voltage swings than is associated with bipolar exponential turn on. The result is an increase in the time required to charge and discharge node capacities, with consequent prolongation of switching times. The scaling of the device conductance by W/L is also seen from (4).

The threshold turn on characteristic is shown in Figure 2-16, illustrating the gate must be at -5 volts for conduction. Figure 2-17 illustrates the drain characteristics. These characteristics are similar to tube characteristic. Hence, the measure of gain used is the transconductance, g_m . Another point to note is that the drain characteristics all go through the origin. This implies zero offset voltages, making the MOS potentially the ideal multiplex switch.

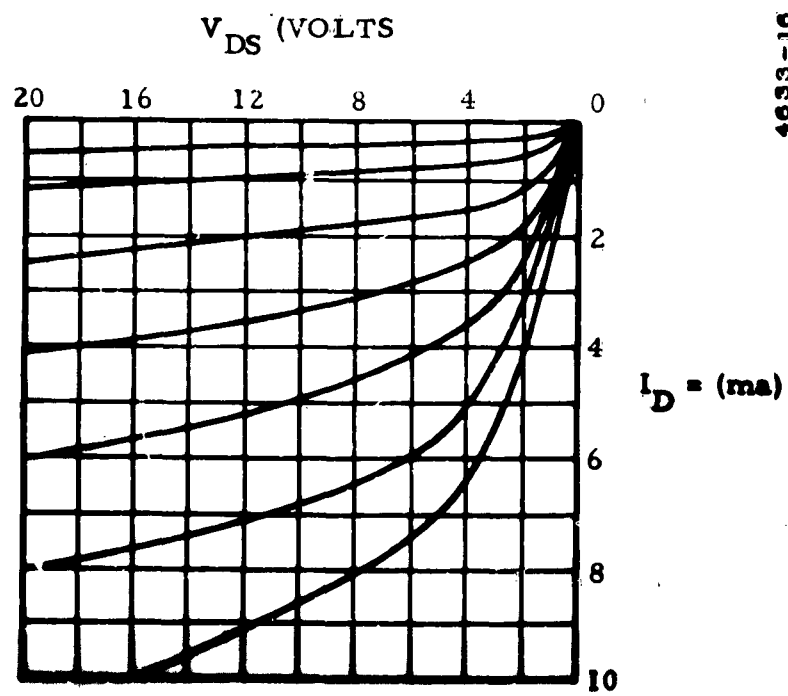


Figure 2-16. Drain Characteristics

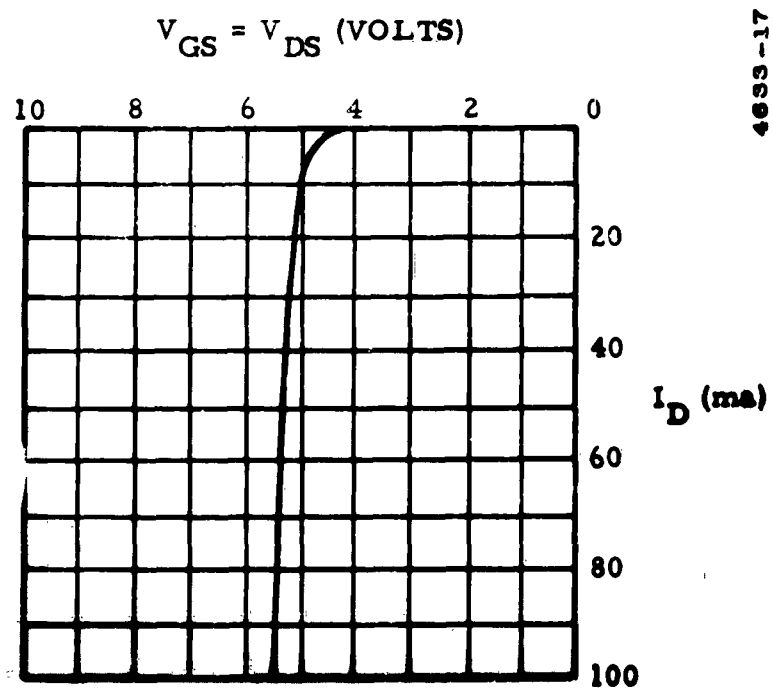


Figure 2-17. Turn-On Characteristics

3. MOS Logic

The basic logic configuration available with MOS, shown in Figure 2-18, include all the requisite Boolean functions. The load resistors shown are actually MOS transistors with conductance scaled down by a factor of 10 or more. Switching speed of these circuits may be calculated as follows

a. Turn on Time

$$t_{on} = \Delta V_{DS} C_{total} / I_{DS}$$

Typical values are $\Delta V_{DS} = 15$ volts, $C_{total} = 10$ pf, $I_{DS} = 5$ ma. Therefore

$$t_{on} = 15 \times 10 \times 10^{-12} / 5 \times 10^{-3} = 30 \text{ n sec}$$

b. Turn off Time

$$t_{off} = 2.3 R_L C_{total}$$

for decay to 90% of the output. With $R_L = 5K$, C_{total} as above,

$$t_{off} = 2.3 \times 5 \times 10^3 \times 10 \times 10^{-12} = 115 \text{ n sec}$$

This is a fundamental limit in the size of R_L . The importance of building low capacitance devices is also evident. The turn-off time requirement is a constraint on fan-out due to the capacity build up as fan-out is increased.

Comparison of MOS and Monolithic Silicon Bipolar Technology

1. Sources of Information

When discussing the claimed advantages of a new technology such as MOS, we must keep in mind that in many cases these are open to dispute. Moreover, the economic and proprietary interests of the semiconductor industry are such that it would be foolhardy to expect dispassionate appraisals either pro or con. In the material to follow the views representative of a wide-section of the industry are presented. A review of the literature and discussions with representatives of leading semiconductor companies shows a surprising concensus in many areas.

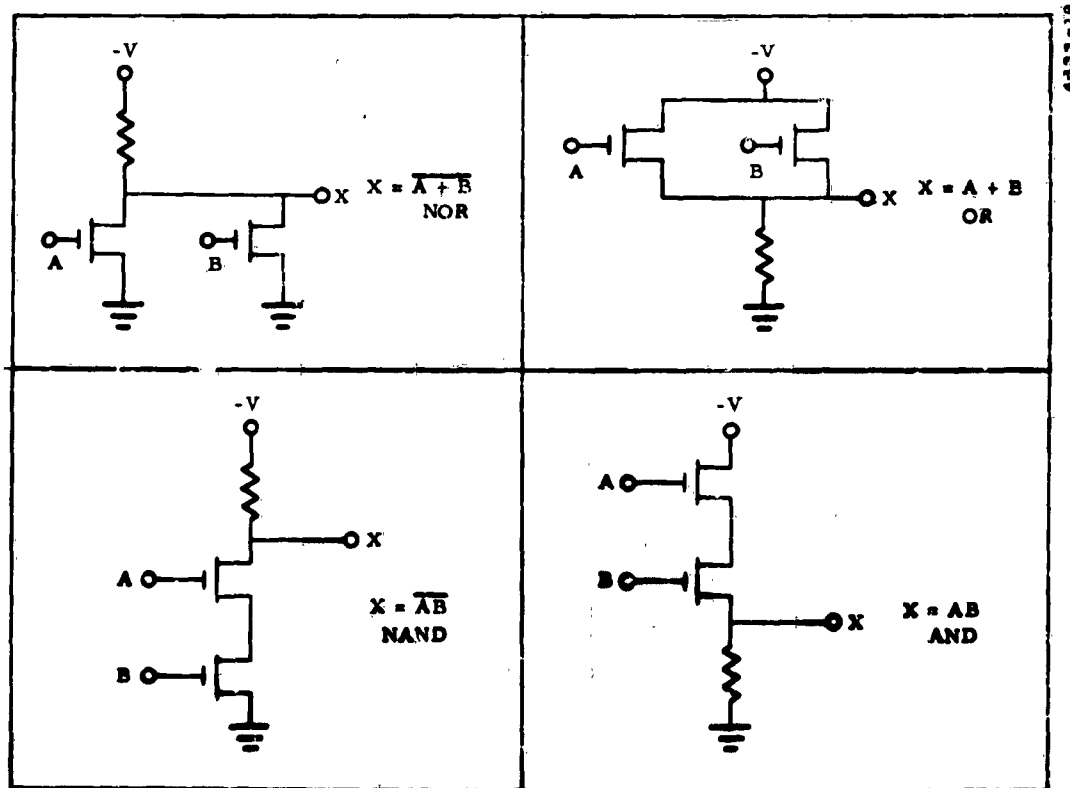


Figure 2-18. Logic Configurations

Litton is also conducting its own program of evaluation and laboratory scale fabrication of MOS devices. Additional evaluation information is available from reports of the Battelle Memorial Institute which has the responsibility for conducting MOS field effect analysis under Navy contract Nav Air Dev Cen N62269-2470.

2. Advantages of MOS

A list of the claimed advantages for MOS are as follows:

- **Simpler Manufacturing**
- **Self Isolation**
- **Small Geometry**
- **Lower Power Dissipation**
- **Superior for Large Arrays**
- **Ease of Circuit Design**

a. Simpler Manufacturing

Unquestionably, large MOS arrays are simpler to manufacture than the more common bipolar integrated circuit arrays. The controversy centers about how much simpler. A basic starting point is the bipolar IC's. It is a fact that these require four diffusions, as follows:

- **N-type Diffusion Prior to the Epitaxial Deposition.**
- **Isolation Diffusion. (All circuit elements on a double-diffused device must be electrically isolated from each other.)**
- **Base Diffusion (also used for resistors).**
- **Emitter Diffusion**

To perform these diffusions and the interconnection of passive and active elements by metalization, 6-7 photolithographic maskings are required.

Now what about MOS? A leading MOS device manufacturer states that only one diffusion and 3 maskings are required. These are used as follows:

- Oxidize n-type silicon wafers
- Photoengrave holes in the oxide to provide windows for source and drain regions.
- Diffuse source and drain regions (p^+ type)
- Photoengrave oxide to provide windows for gate, drain, and source metalization.
- Deposit gate, drain, and source contacts by evaporation of Aluminum.

This process can also simultaneously provide the load resistors required by logic circuitry. An MOS transistor with the proper width to length ratio and with the gate connected to the \bar{c} functions approximately as a resistor.

However, to obtain reasonable circuit performance, somewhat greater process complexity is involved. For one thing, an additional masking is required to deposit a thinner oxide layer (1000 \AA) over the gate than over the remainder of the device. This is necessary to insure adequate conductance in the "on" state. Additionally, a second diffusion of phosphorus is normally used because of its stabilizing effect on the oxide. Thus, the complexity is now increased to 2 diffusions and 4 maskings - still superior to bipolar IC's by almost a factor of two.

However, the comparison is still not entirely valid. The bipolar IC's used for the comparison employ isolating techniques such as buried layers or dielectric (oxide) layers to achieve switch speeds as typified by the following:

	<u>Discrete Circuit</u>	<u>Monolithic IC No-Buried Layer</u>	<u>Monolithic IC Buried Layer</u>	<u>MOS</u>
Turn on time, ns	16	26	20	30
Turn off time, ns	26	38	34	100
Propagation Delay	10	16	13	

Thus, a diffusion and masking step could be eliminated from bipolar IC processing and still achieve speeds comparable to MOS (see discussion

on Operation of MOS). The MOS processing advantage is now diluted to one diffusion step and one masking step.

In summary, the controversy over relative processing complexity is difficult to resolve because processing details are legitimate trade secrets.

b. Self Isolation

Self isolation refers to the capability of operating in close proximity to like devices without degradation due to passive and active interactions. This is unquestionably an important advantage of MOS. As can be seen by Figure 2-14, each junction is operated back biased - in other words, in a high impedance state. In effect, the source, drain, and gate are electrically isolated from the substrate. This characteristic is ideal for the fabrication of total logical subfunctions and complex arrays on the chip as it permits extremely close packing density. As an example, a 100 bit shift register requiring over 600 active devices has been fabricated on a die area of 65 x 100 mils. In the bipolar IC's, approximately 30 percent of the die area is used to provide the required electrical isolation.

c. Smaller Geometry

MOS transistors on large arrays average about 2-1/2 square mils in area. This extremely small size is due to the fact that the MOS may be scaled down in size without performance degradation, provided the load capacity is similarly scaled down. An explanation of this fact is that the gain of the device, g_m , is a function of the ratio of the width to channel length. If these are reduced in the same proportion, the g_m is unaltered. (This is not the case for extreme reduction in size, say below 2 mils. Below this figure, bonding pads, for example, begin to occupy a disproportionately large percentage of the chip area.) Another factor favorable to size reduction is the high input impedance (10^{15} ohms) implying a negligible drive requirement, and consequently, a driving source of low current capacity.

The bipolar transistor on the other hand, has a direct relation between area and β , the current gain. Moreover the input impedance is low, typically of the order of several thousand ohms. For reasonable β , an area of 20 square mils is required. If to this we add a 30 percent penalty for isolation, we get a figure of 26 square mils per bipolar transistor.

The advantage to MOS, thus, is in the ratio of 10:1. We may examine this another way in terms of the following table showing the area requirements of a flip flop in bipolar technology vs. a 20-bit MOS shift register*.

<u>Year</u>	<u>1 J-K Flip-Flop (Bipolar)</u> <u>Die Size, Mils</u>	<u>20-Bit Shift Register (MOS)</u> <u>Die Size, Mils</u>
1965	40 x 40	44 x 44
1966	30 x 30	
1967	25 x 25	

Again, the advantage to MOS appears to be of the order of 10:1, taking into account the higher complexity of the J-K Flip Flop vs. a shift register stage. One can find all sorts of geometry ratios of MOS to bipolar in the literature. These range from 1:25 to a grudging 1:2. However, the above cited table for bipolar are the projections of a leading bipolar manufacturer and the 20-bit shift register is available commercially.

d. Low Power Consumption

In the conventional operational mode, MOS demonstrates low power dissipation because of the inherently high input impedance and low input capacity. This permits relatively large drain resistance to be employed if only modest switching speeds are required. A spectacular decrease in the standby power is achieved through the use of complementary logic comprised of n-channel and p-channel devices connected in series. The n element acts as a load for the p element. Because one device is always off when the other is on, essentially zero power is consumed in the standby state. It has been calculated that 10^7 complementary logic gates would consume less than 1 watt of standby power! This is in contrast to bipolar complementary logic which requires base current drive while in the standby mode.

A characteristic of low power bipolar logic is the fact that it is generally limited to low speed (less than 100 kc). The complementary MOS has been demonstrated to have propagation delays of less than

*Data for J-K Flip Flop adapted from IEEE Spectrum, pp 67, June 1964.

100 nanoseconds. Moreover, fanouts as high as 50 can be used because of the large input resistance with the propagation delays still maintained below 1 microsecond. The large fanout reduces the number of logical levels required, and hence, the associated propagation delay.

e. Superior for Large Arrays

This follows directly from the preceeding discussions on small geometry, high fanout, and low-power consumption. Another factor is that in complementary logic, resistor tolerance problems are not encountered, permitting higher temperature differentials between the conducting and non-conducting elements. Cooling problems are minimized as well.

With respect to ease of interconnection on the array, the MOS has a further advantage. Because of its high input impedance, it can tolerate interconnects of p diffused strips as well as the more typical alumina deposition.

f. Ease of Circuit Design

One familiar with the complex circuit calculations required in bipolar circuit design can best appreciate the relative ease of circuit design with MOS. The following factors contribute to easier circuit design:

- Fan-in and Fan-out are essentially unlimited.
- Series or parallel logic may be flexibly employed as required.
- Direct coupling from gate to gate is employed.

It will be recalled that in bipolar design, fan-in and fan-out variations are one of the chief design constraints. Freedom from this constraint is due to the essentially infinite impedance of the MOS.

The latter two factors obtain because of the high threshold of the device for turn-on (5-6 volts). This permits series logic to be employed as desired and additionally, eliminates the coupling circuit necessary with bipolar circuitry. However, series logic is costly in die area. To

1000

In the interest of achieving maximum circuit complexity on the chip, the series circuit configuration should be avoided unless justified by other considerations.

These three factors, in conjunction, essentially imply that the user is relieved of the requirement of basic circuit design for standard applications. However, much work remains in connection with special requirements such as high speed switching using current mode logic.

3. Disadvantages of MOS

The major disadvantages of MOS with respect to bipolar, monolithic technology is speed. As indicated above, bipolars are characterized by switching speeds of the order of 10 nanoseconds, whereas MOS is in the 100 nanosecond range.

This may or may not be a system disadvantage, depending on the logic design. The highly parallel computing structures that can be exploited with the new batch technology do not place a premium on device speed. This in contrast to the previous limitations of discrete circuit technology, where sheer bulk often demanded the maximum speed of each gate.

The basic reasons for slower MOS speeds are due to the following factors:

- The large swing (3-5) volts implies longer charging-discharging times for the nodal capacities.
- Conduction follows a square law, in contrast to the exponential diode law for bipolars.

Because MOS is a majority carrier device, speed is limited principally by RC time-constant considerations rather than transit time or minority-carrier storage effects. As implied in the preceeding discussions, new MOS circuit types of high speed will undoubtedly be available at the cost of less component density.

2.1.4 Summary and Conclusions

Borrowing the jargon of the commercial computer field, the current vintage of avionics computers may be characterized as third generation.

This generation is distinguished particularly by its employment of monolithic integrated silicon circuits. Perhaps erring on the side of conservatism, monolithic IC's will be the mainstay of production avionics computers up to and including 1969-1970.

The post 1970 computer generation will feature monolithic arrays incorporating up to 1000 transistors. This will make feasible the realization of the logic requirements of a digital computer on a 1 inch diameter silicon wafer. The technologies most vigorously contending for this application are the MOS and further advancement of the bipolar silicon art.

2.1.5 Bibliography for Sub-section 1.1

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2.2 MEMORY SELECTION FOR AVIONIC DIGITAL COMPUTERS

The memory system for current avionics computers is structured in a multi-level configuration. One level provides for the storage of program instructions and constants. Size of this level may range up to 32,000 words, but in the usual application a more likely range is between 4000-8000 words. A second level of memory, called the scratch pad, provides for the storage of intermediate results of computation. The capacity usually varies between 100-1000 words. A third level of memory is frequently provided for bulk storage of test and maintenance routines which may be called into the main memory by block-transfer commands.

A distinguishing feature of the first-level memory is that it has (heretofore at least) employed non-destructive readout (NDRO) to eliminate the possibility of permanent program errors due to intermittent writing errors. This technique has the further advantage of minimizing the amount of equipment required in the airframe through the elimination of write-in electronics. The scratch pad has typically been a DRO core memory with read-write cycle times of the order of 1-2 μ s. The third level differs significantly in access time requirements, with the result that more economical storage media may be employed. Storage capacities up to 50×10^6 bits (approximately 2×10^6 words) may be provided using magnetic tape in a small package at data rates of the order of 100kc/s.

The performance and cost of a digital computer complex for avionics systems is greatly influenced by its memory. Selection of the appropriate memory requires the analysis of a wide ranging technology. In this selection the designer must also consider basic system requirements, performance parameters of candidate memory systems, costs, and availability. A review of the pertinent factors will be presented herein.

2.2.1 Basic Requirements

The memory system specifications for avionics digital computers are stipulated in terms of capacity (number of words), size, speed, environment, and reliability. Capacity requirements stated above are typical for the great majority of avionics systems. With respect to size, the volume constraints on the complete avionics computer is usually less than one cubic foot. A reasonable allocation to the memory is 50 percent of the computer volume. Advances in logic packaging densities make it unlikely that this ratio can be attained unless new innovations in memory are devised.

With respect to speed, environment, and reliability, the following considerations are pertinent:

Speed

Two factors determining memory speed requirements are:

1. System computation requirements
2. Logic speed vs. memory speed.

Typical avionic system computation requirements are shown in Table . The resultant range is 100,000 to 200,000 instructions per second. In terms of execution times for short instructions, which is the reciprocal of the above, we get 5 - 10 μ s.

Indexed instructions normally require three memory accesses. From this we can deduce the equivalent memory speed requirements of 1 - 2 μ s. These speeds may also be compared with logic delays. For example, TTL (transistor-transistor logic) gates of 30 - 40 nanosecond pair delay, and DTL (diode-transistor logic) gates of 50 - 60 nanoseconds are commonly available. To fully exploit logic speed, therefore, memory speeds below 1 μ s are definitely desirable.

The factors entering into the determination of memory cycle time are given by¹

$$T = 2t_s + t_g + t_n + t_a + t_t$$

Here $2t_s$ is the time required to switch the memory element twice (as is the case in DRO memories); t_g is the sense amplifier delay; t_n is the transient decay time before the memory can be re-accessed; t_a is the memory address time; and t_t is the signal propagation time in the digit windings. These parameters will now be examined.

¹J. A. Rajchman, Computer Design, September 1963

TABLE II-4

Problem Dynamics	Iterations Per Second	Length of Instruction Loop	Total
High	100	500 - 1000	50,000 - 100,000
Intermediate	10	1000 - 6000	10,000 - 60,000
Low	1	1000	1000

Switching Time

Switching time of the memory element is a function of the drive, the memory organization, and the material. The switching time decreases with faster rise time and higher intensity of drive. The range of drive currents has been from 100 ma to 1 amp, the upper limit being associated with film type memories. With respect to memory organization, word organized are faster since no limit on the drive is imposed such as the half-select requirement in coincident current selection.

Permalloy films exhibit switching in a few nanoseconds (ns) whereas the fastest ferrites switch in approximately 25 nanoseconds. Ferrites must be shaped to minimize the length of the flux path by using micro-miniaturization techniques to achieve such speeds.

To date, no known avionic memory has exhibited speeds approaching these due to inherent difficulties of cross talk at the high rise, high amplitude drives required. The typical cycle time of avionic memories is 1 - 3 μ s.

Sense Amplifier Delay

A multi-transistor sense amplifier is required to bring the memory signal from the millivolt level to the logic level (volts). The amplifiers contribute delays of the order of 10 ns due to inherent transistor delay phenomena.

Transient Decay Time

In DRO memories, the necessity to rewrite the accessed information introduces large "disturb" signals on the sense lines. Despite the use of sophisticated cancellation schemes, delays are entailed to allow the "disturbs" to decay to an acceptable level. These delays are in the range 10 - 20 percent of the total memory cycle time.

Memory Address Time

This is a small delay, of the order of 20 nanoseconds, imposed by propagation time of the decode logic.

Signal Propagation Time

The drive and sense windings of the memory are transmission lines with finite propagation time. Design criteria are imposed to minimize the length of the transmission path.

Environment

The environment to which avionics is subject represents another major departure from ground based systems. Shock, vibration, and humidity immunity has been attained through extension of known art whereas performance over the temperature range from -40° to 100°C has required new materials research. The switching characteristics of conventional cores are affected by temperature to a degree that operation within narrow temperature range (15° to 55°C) has been required. Even this narrow range required thermal and drive current compensation. These problems have been overcome through new materials having the requisite square loop properties and Curie temperatures above 600°C. This has been accomplished in cores using lithium-ferrite compositions and in thin films with permalloy compositions (81.5 percent nickel and 18.5 percent iron typically).

Reliability

The disastrous consequences of loss of memory in an avionics system has heretofore resulted in different configurations for the avionic memory as contrasted to ground based systems. One result of this problem has been the employment of NDRO in the avionics computer for all program and constant storage; and DRO for scratchpad requirements. With the

recent trend to high reliability memory systems, the need for two different memory types is being seriously questioned for the first time. Moreover, the memory performance may be continuously monitored by including redundant bits in the word. On detection of a fault, the program may be reintroduced from a bulk store in a few seconds.

Mean time before failure performance in avionic computers is now frequently a contractually stipulated item. Computer design currently in progress are committed to achieve on the order of 7,500 hours MTBF and higher by 1969-1970. The required memory system reliability is seen to be greater than 10,000 hours. Where necessary, redundant memory banks are being employed together with memory performance monitoring.

2.2.2 Ideal Memory Characteristics

We have discussed the desired characteristics of the memory for an avionics computer in terms of capacity, speed, insensitivity to environment, and reliability. Additionally, other qualifications must be imposed to fulfill the description of an "ideal" memory element. These include:

High Output Signal-to-Noise Ratio

A rate in excess of 5 to 1 and an absolute output signal magnitude greater than 10 millivolts is desirable for ease of sensing and simplicity of the sense amplifier.

Simple Selection

The efficient selection of coincident current organization is desired. This can nearly be attained even for an NDRO, word organized system by increasing the number of words addressed simultaneously and interposing gating to select only the desired word. In the DRO case, a trade-off is involved between the greater complexity and cost of linear select and the higher speeds it affords.

High Storage Density

Avionic applications impose severe size and weight constraint. Effective densities of 1000 bits per square inch are desired whereas current practice approaches approximately 400.

Low Power

Current drive required by available magnetic memories range between 200 to 1000 milliamperes. An order of magnitude reduction is desirable but will probably simultaneously reduce output. The advent of higher density packaging will reinforce the drive to reduce power in order to minimize heat generation problems.

Low Cost

Automation of fabrication techniques has resulted in lowering of costs for avionic memories. However, the 1 cent/bit goal is far off (by several orders of magnitude). Batch processes should reduce costs to this level ultimately. Integration of the select, drive, and sense circuitry with the plane using completely automatic techniques represents the ambitious goal of batch fabrication.

2.2.3 State of the Art in Computer Memories

This section describes memory systems used in state of the art avionic computers. These systems may include an NDRO memory, a coincident current DRO memory, a low cost NDRO (core rope) memory, and a multi-track tape memory. Performance parameters of these storage media and known application examples will be given in the material to follow.

NDRO Memory

1. General Considerations

NDRO storage is used for permanent storage of the basic computer program, subroutines and constants. The permanent program stored in the NDRO section is nondestructively interrogated, ie, during the readout process, no rewriting is required as in conventional DRO memory. Also, the program data stored in the NDRO section are completely unaffected by a loss of power or other external transients. A further advantage of NDRO is the higher operating speed achieved through elimination of the rewrite requirement after each readout.

A detailed evaluation of the various electrically alterable NDRO storage devices, memory organizations, selection techniques, etc, indicates two that are in current use for avionic computers: the two-hole MAD (multi-aperture device) based on flux mode switching and using linear selection;

and the thin film bicore memory, also using linear select. While these techniques are not an ultimate solution to airborne NDRO memory requirements, the continuing improvements in size, weight, power, cost and producibility also makes them the most probable choices for a state of the art design. In particular, in the MAD type NDRO significant design improvements in organization, winding, assembly techniques, and the application of microelectronic circuits has further reduced size, weight, power, and cost.

Figure 2-19 shows a complete 4096 word (24 bit) self-contained memory module using MAD. The design features of note are:

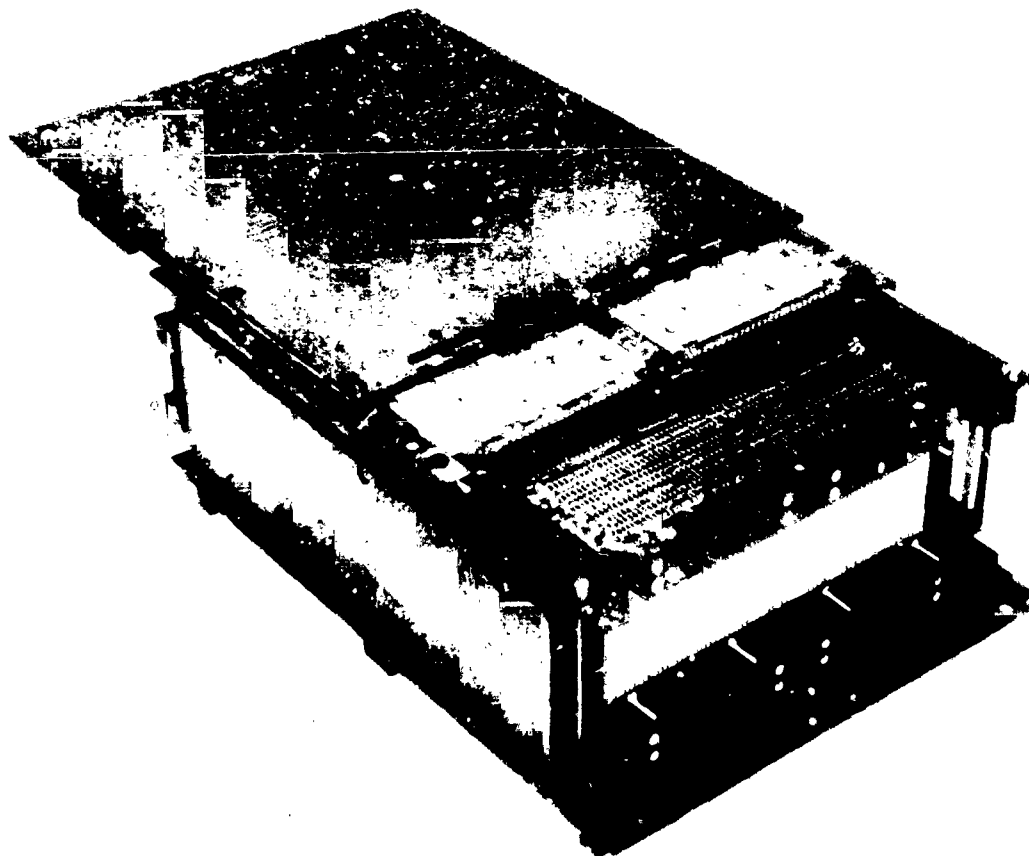
1. Linear selection is used for reliable operation at high speed and under severe environment
2. Micro-electronic design is used throughout
3. High signal to noise ratio in excess of 10:1 is attained.

Weight of the complete assembly is under 15 lbs. Cycle time is 1 microsecond.

Figure 2-20 shows a block diagram of the memory. Reading is accomplished by providing a magnetizing force of 400 milliamperes-turns. With drives of this magnitude, a large, relatively fast read signal is induced in the sense line if the core being read had stored a "one". An NDRO "one" is approximately 220 millivolts in amplitude (open circuit).

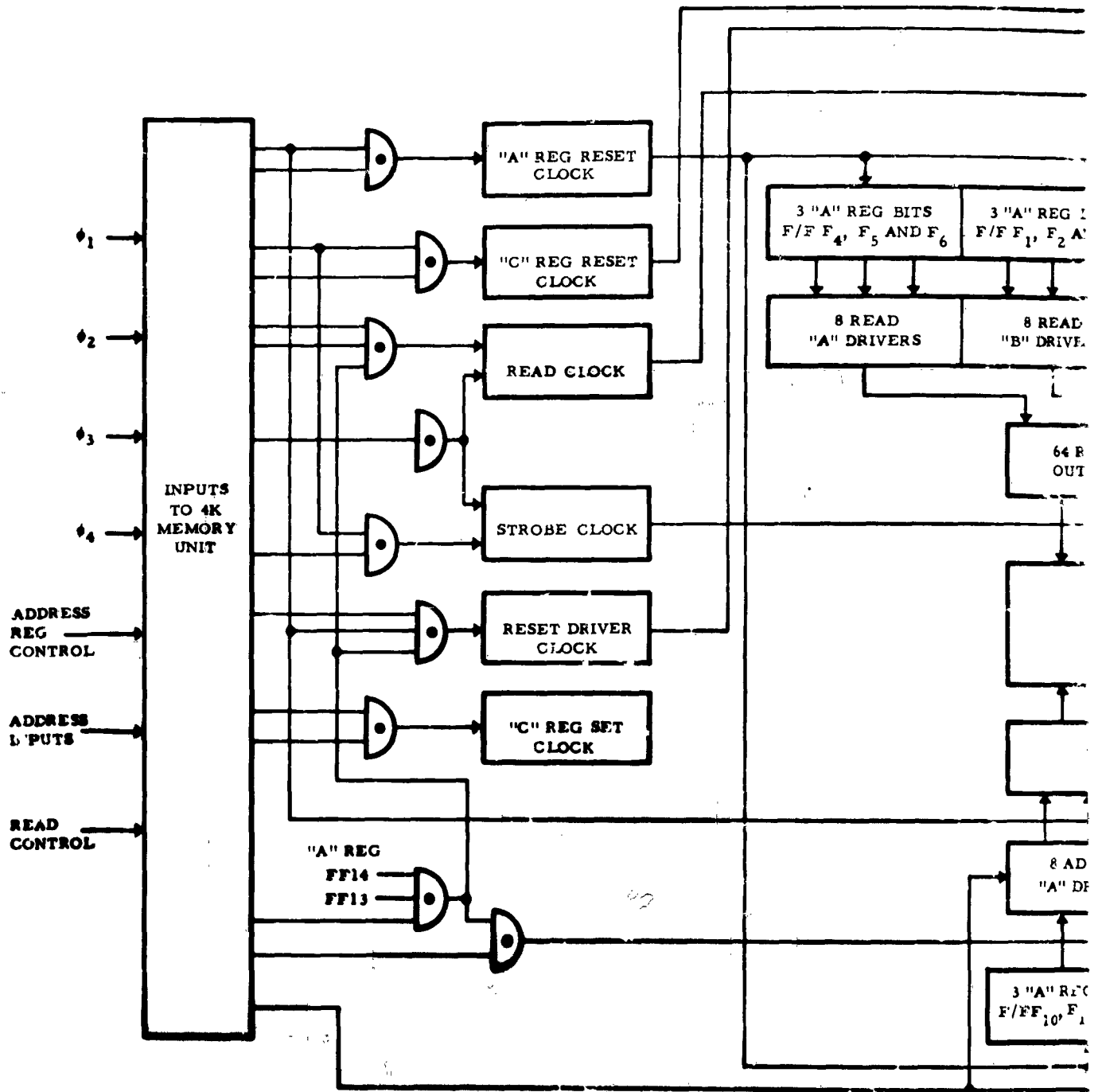
If the core is in the "zero" state, a nondomain wall movement type of disturbance is produced. This disturbance is short in duration and small in amplitude. The "zero" output, of the NDRO core is less than 20 millivolts in amplitude. Because of the high "one" to "zero" ratio, and the fact that the sense line links only the cores of the selected word, a large signal-to-noise ratio is obtained.

A word in the storage matrix is accessed by storing the binary address of that word in a 14-bit binary register. The register outputs are then decoded to select an address switch. In turn, the address switch selects a particular plane in the storage matrix and the read line drive associated with the addressed word. The sense amplifier is gated on during the read time. Only the "one" voltage generated by the cores switched at read time will be of sufficient amplitude to overcome the threshold level that has been preset in the sense amplifier. Therefore, "ones" will be amplified, and in turn the appropriate output register bits will be set.



0000-02

Figure 2-19. NDRO Memory Module



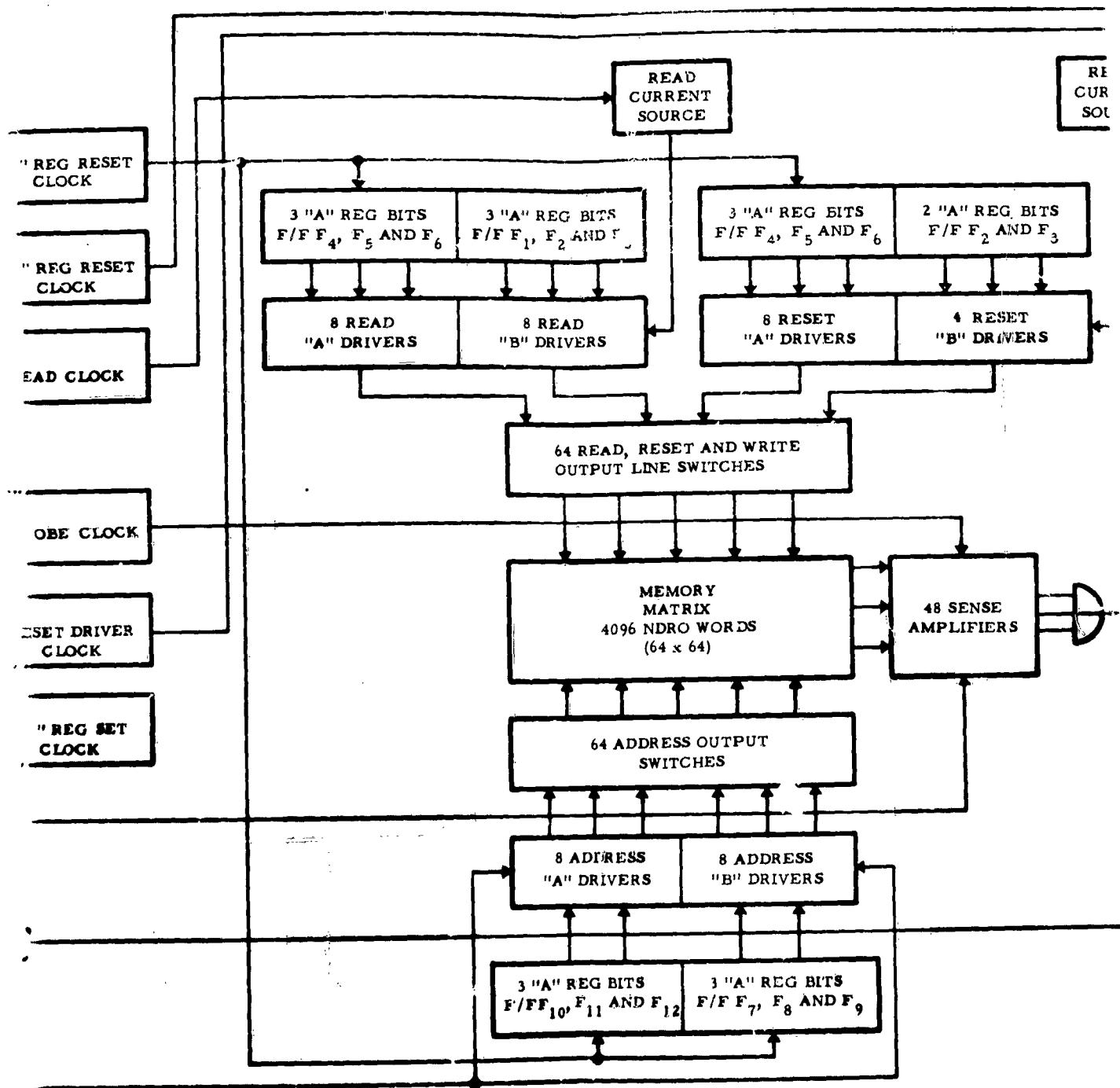


Figure 2-2

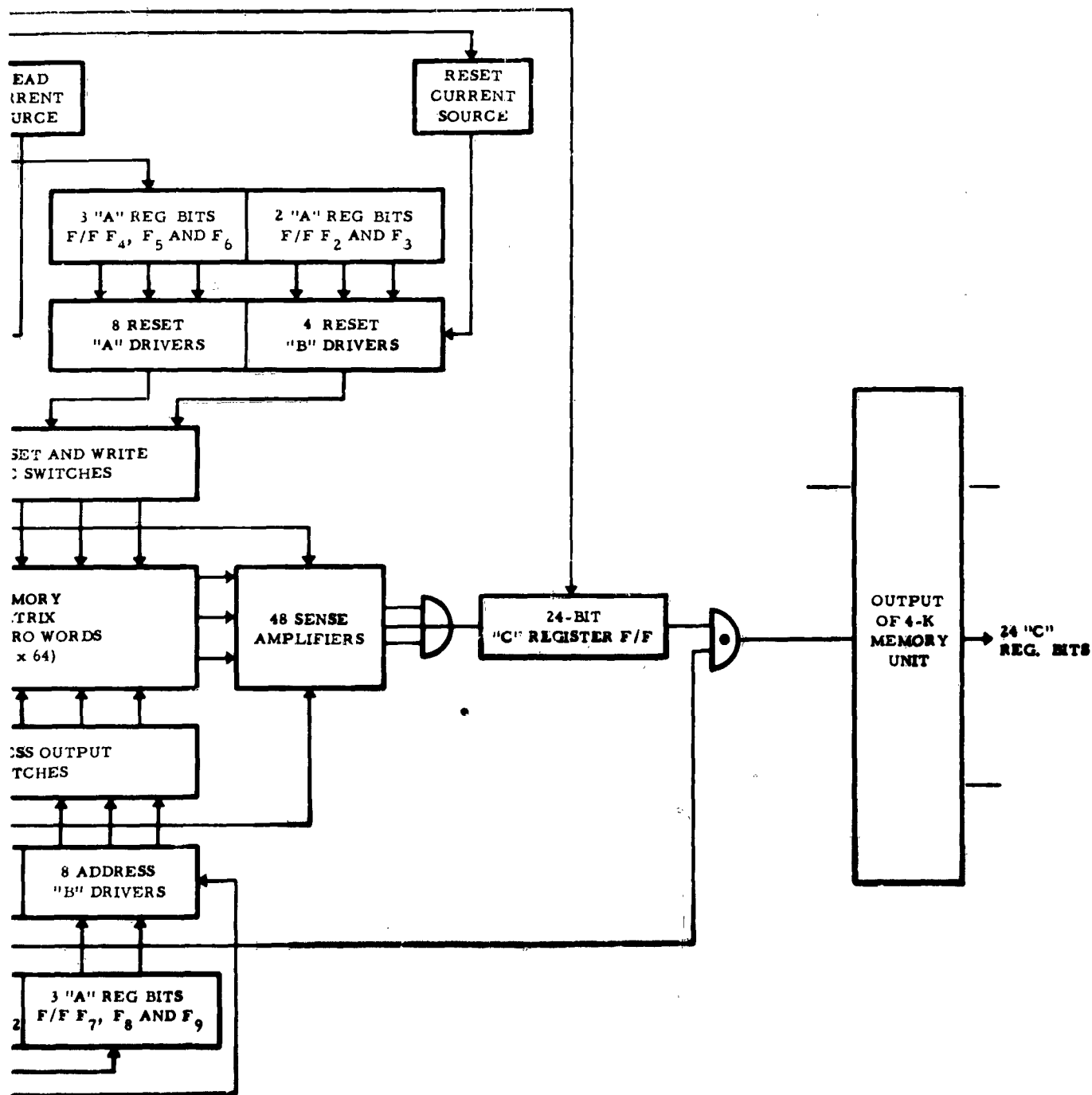


Figure 2-20. NDRO Block Diagram

C

A reset operation which uses circuits similar to those used for the read operation follows each read operation. The reset or prime current flows in the word direction and is therefore not bit-dependent. The reset current will reset the flux in a core that was set to the "zero" state. (The flux-steering characteristics of the multi-aperture core used as the NDRO storage device are described below).

The various clocks and control terms that are required for memory operation are for the most part generated by employing monostable flip-flops controlled by the computer multiphase clock. Figure 2-21 shows the relationship between several of the clock and control terms for an NDRO read operation. The shaded areas at the front and back edges of all memory clocks indicate the variation in clock width that could occur under multiphase clock jitter, component delays, etc. The memory timing system must be designed to yield satisfactory timing signals under worst-case conditions.

Storage Cores

The core memory stack consists of 4096 words of nondestructure readout storage. The device used for this storage is a rectangular (98 mils by 86 mils) multi-aperture ferrite core. Figure 2-22 shows the MAD with the associated windings to perform the clear, write in, interrogation and sensing of the selected memory location. A single turn clear line is applied through the large hole. The current I_{CL} sets the flux in the entire MAD and establishes the clear condition in the device. The arrangement of having the write line thread both holes results in an optimum constant flux reversal during the process of writing a "one" into the MAD.

Figure 2-23 shows the readout signal interrogated and sensed in the small hole as a function of the write current. The graph indicates clearly the desirable characteristics of this write-in technique. The advantages include avoiding disturbance of the large aperture and providing constant flux reversal during the write time, thereby making the device relatively insensitive to temperature and power supply variations.

In an NDRO memory system, a restoring of the extracted data from the core is not required as is the case for conventional DRO memory systems. However, the flux reversal caused during the interrogation process must be reset by dc bias common to the entire storage matrix or by a linearly applied pulse in the opposite direction to the original

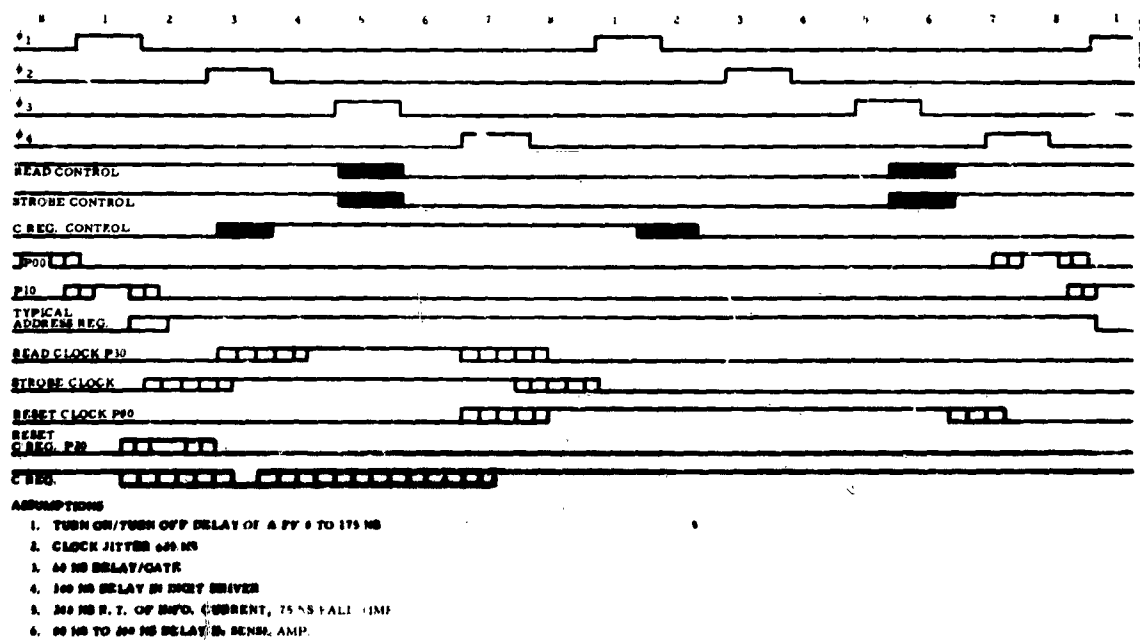


Figure 2-21. NDRO Timing Wave Forms

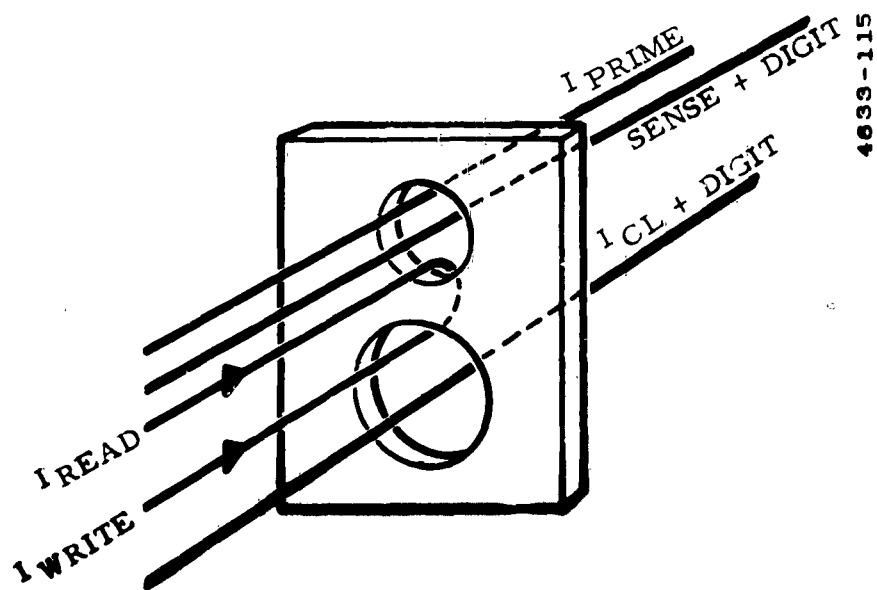


Figure 2-22. Winding Configuration For the MAD

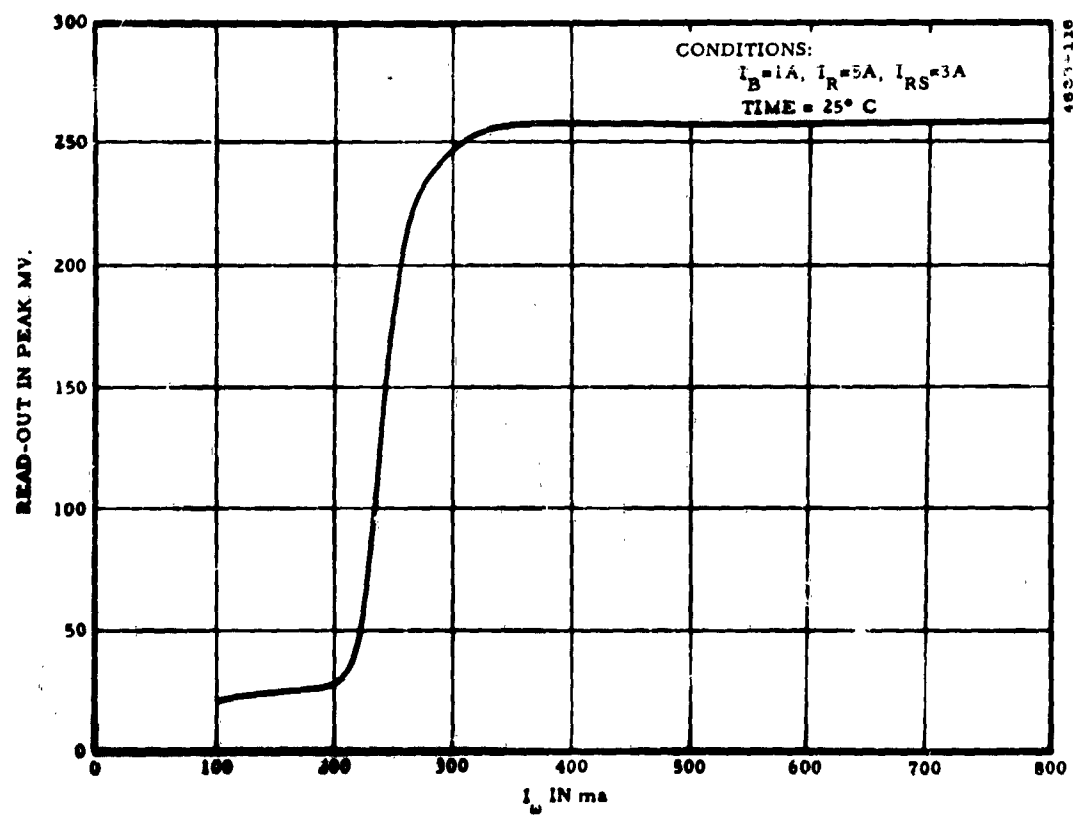


Figure 2-23. Readout Signal as a Function of Write Current

read current. Additional reliability in regard to the flux relationship in the MAD or in case of power failure is gained by using the first read pulse through the small aperture as the "prime pulse". The following current pulse, of opposite polarity, is then used as the actual readout pulse.

During the write cycle, full write current cannot be applied, and some means of writing "ones" and "zeros" into the MAD must be devised. Therefore, during the write cycle a current of $2/3 I_W$ is applied through the core in the word direction. If a one is to be written in the core, this current is reinforced by the information current $+ 1/3 I_W$. If a zero is to be written in the core, the current I_W is opposed by the information current which is applied in opposite direction to that of I_W . The bi-lateral information current of $\pm 1/3 I_W$ which operates in conjunction with the write current I_W , effectively establishes the data written into the core over a wide variation in current amplitude.

2. Memory Circuits

The memory system shown in Figure 2-19 has been constructed using four microelectronic flatpacks as the major building blocks. The building blocks used are as follows:

- a. Logic Gate - A dual four-input integrated circuit NAND gate.
- b. Sense Amplifier - A monolithic differential sense amplifier.
- c. Transistor Pack - Four discrete, planar, epitaxial, high-speed NPN transistors in an integrated circuit flatpack.
- d. Resistor Pack - Eight thin-film resistors deposited on an alumina substrate and packaged in an integrated circuit flatpack.

Figure 2-24 shows the integrated sense amplifier, a four-transistor flatpack, and a thin-film resistor pack. Figure 2-25 shows these packs mounted on a memory laminate.

3. NDRO Film Memory

NDRO thin film memories are also available for avionics application. A recent form of film memory consists of layers of iron-nickel and iron-cobalt separated by silicon monoxide. Figure 2-26 shows a single memory

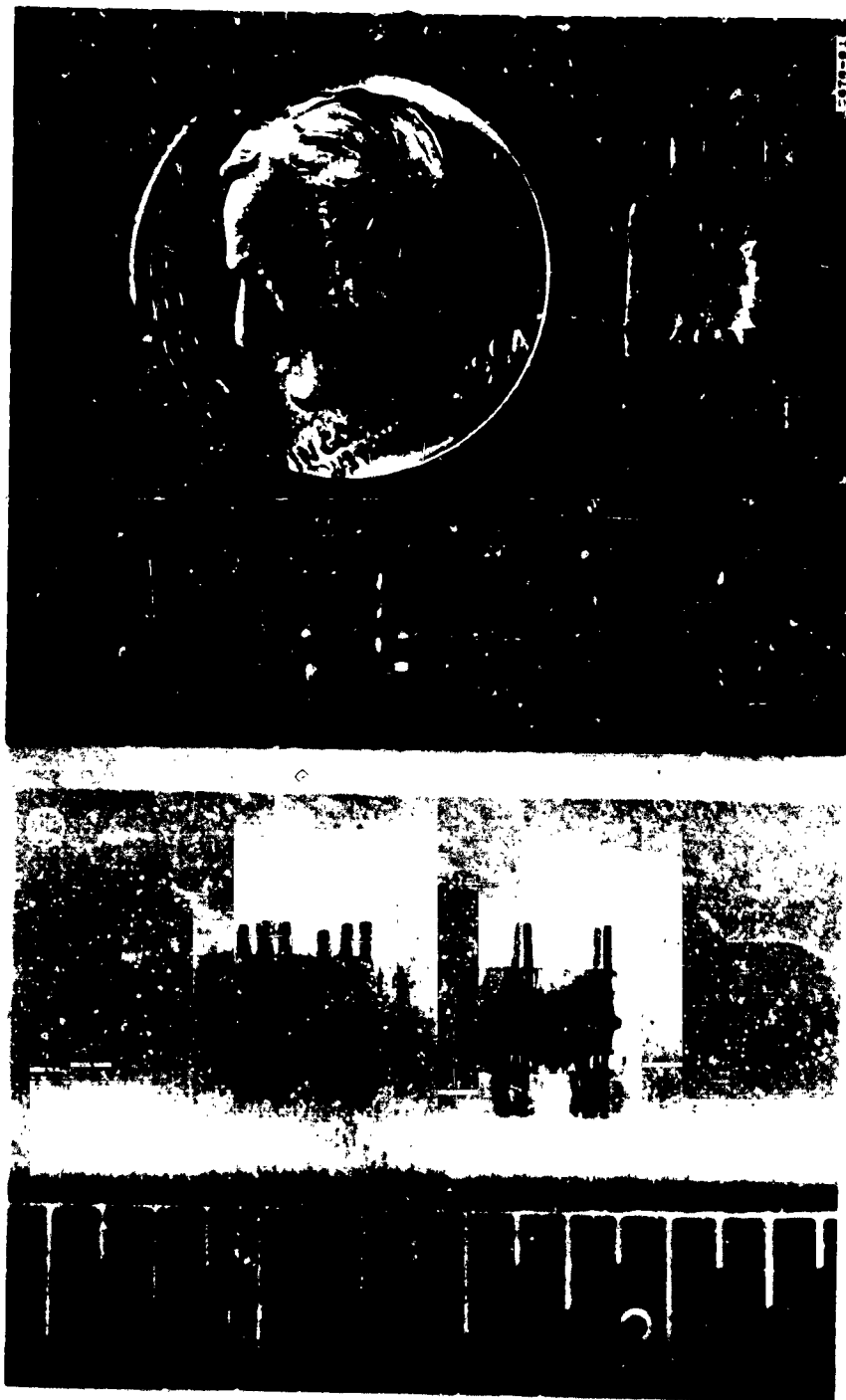
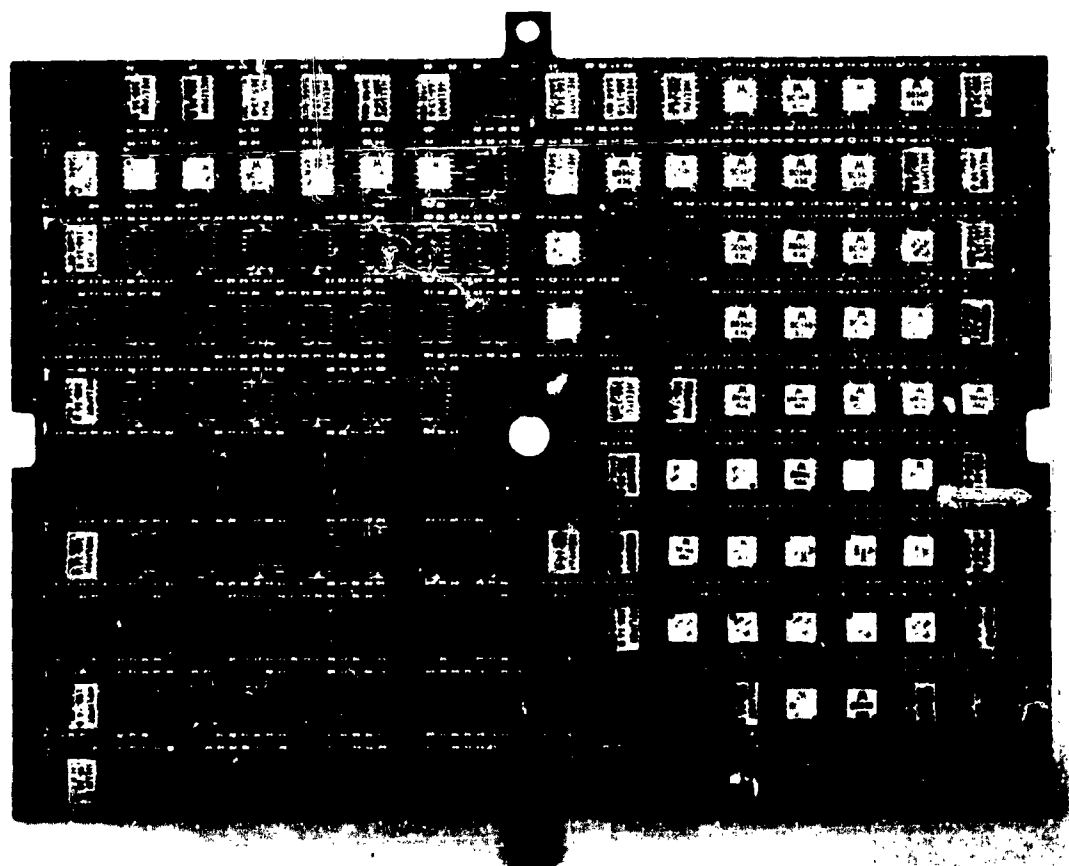


Figure 2-24. Microelectronic Elements



3676-79

Figure 2-25. Memory Laminate

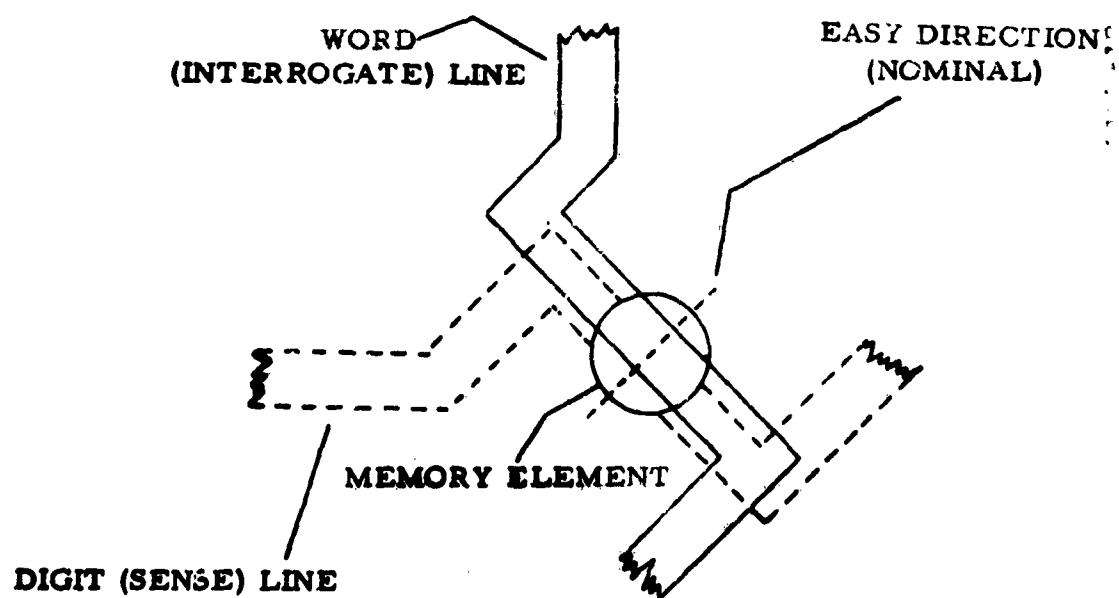


Figure 2-26. Geometry of Word Digit Lines For Film Memory

element and the word interrogate and digit/sense strip lines in the vicinity of the memory element. The layers form, in effect, a single film core that can be magnetized in either of two remanent states. The binary storage capability is a result of the so-called "uniaxial anisotropy" property of thin films fabricated from $\text{Co} - \text{Fe}$ or permalloy ($\text{Ni} - \text{Fe}$). Such films exhibit a preferential or "easy" axis which is used to represent the "1" and "0" states; and a hard axis at 90° to the easy axis, in which direction a field is applied either to interrogate during READ or to serve as one of the two field components required during WRITE. These properties are shown in Figure 2-27.

Storage of information is accomplished by the iron-cobalt layer while readout is sensed through the low-coercivity iron-nickel film. The result is a film pair which can be sensed nondestructively. Binary data is stored in the $\text{Co} - \text{Fe}$ film (called the storage film) during a write operation. The external (demagnetization) field of this film saturates the paired $\text{Ni} - \text{Fe}$ film element in a direction as determined by whether a "1" or "0" has been stored. Thereafter, read-only operation is used (writing is slower than read by a factor of 1000/1, therefore, it is usually never used during system operation). During read, the interrogate field applied is of such magnitude as to switch the read film if a "1" has been stored, thereby producing an output signal on the digit-sense line. After subsidence of the read field, the external field of the undisturbed storage film restores the read film to the "1" state. If, however, a zero has been stored, the read field only drives the read film further into saturation and no output is produced.

Figure 2-28 shows the hysteresis loops associated with the films (not to scale). The external field of the storage film exceeds the coercivity and demagnetization field of the readout film by one-third. The minimum read field to switch the read film is given by

$$H_R (\text{min}) = H_{DS} + H_{CR} + H_{DR}$$

where H_{DS} = external demagnetizing field of storage film

H_{CR} = coercivity of read film

H_{DR} = external field of read film

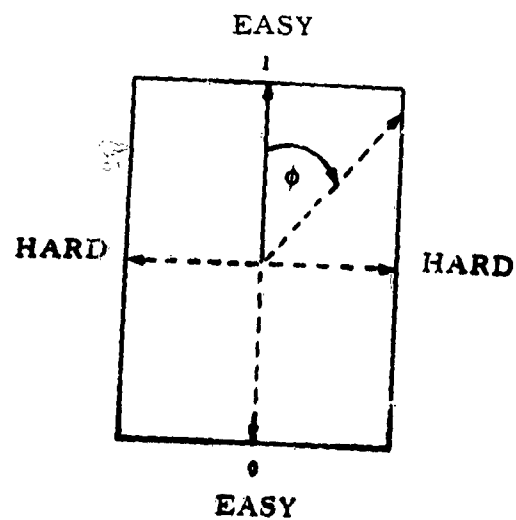
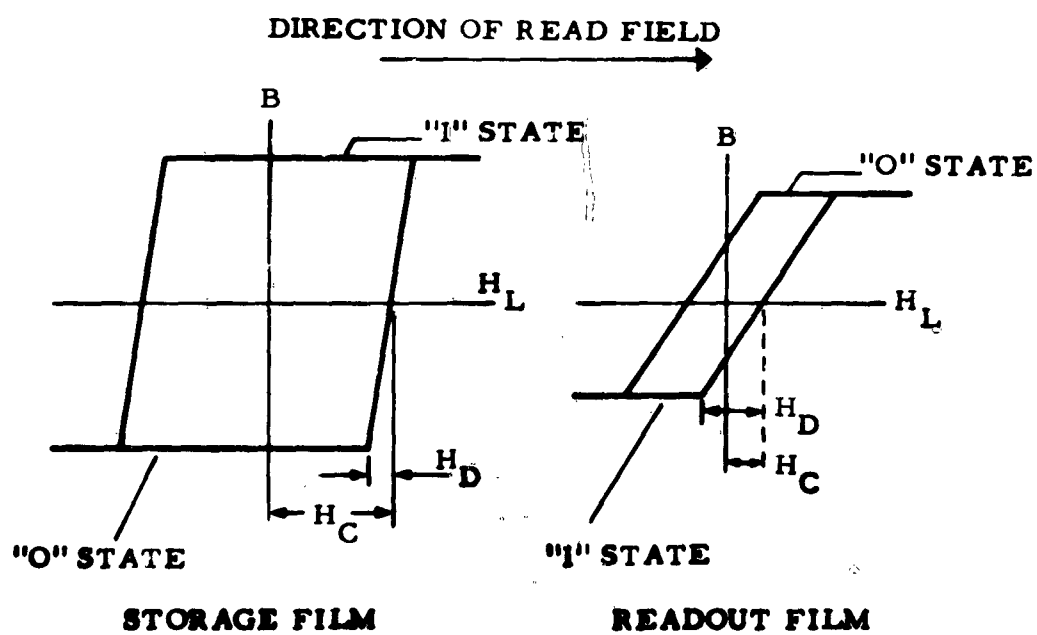


Figure 2-27. The Uniaxial Magnetic Film Preferred and Hard Orientations



4693-21

Figure 2-28. Stylized Hysteresis Loops

The maximum read field that will begin to switch the storage film is given by

$$H_R (\text{max}) = H_{CS} - H_{DS} + H_{DR}$$

where H_{CS} is the coercivity of the storage film and H_{DS} its external field. Thus, it is seen, that ample margin exists between these two conditions.

Waveforms applied for the write operation and the read operation are shown in Figure 2-29. During write, a bipolar pulse is applied to the word line. The digit pulse, with polarity dependent on whether a "1" or "0" is to be written is applied to the digit-sense line. The digit pulse "brackets" the word line pulse in time and is of the order of 1/3 the word line pulse. It therefore adds to one phase of the bipolar word pulse and subtracts from the other phase, with the result that the field representing the digit to be written is twice the magnitude of the "disturb" field. During the read operation a pulse is applied to the word line. The pulse has a negative portion to assist resetting of the film. Only those "elements" storing a "1" produce an output.

The following represents an example of a late state of the art film memory packaged for avionic application.

6912 words, 24 bits/word (6656 words NDRO; 256 words DRO)

3.0 microsecond cycle time

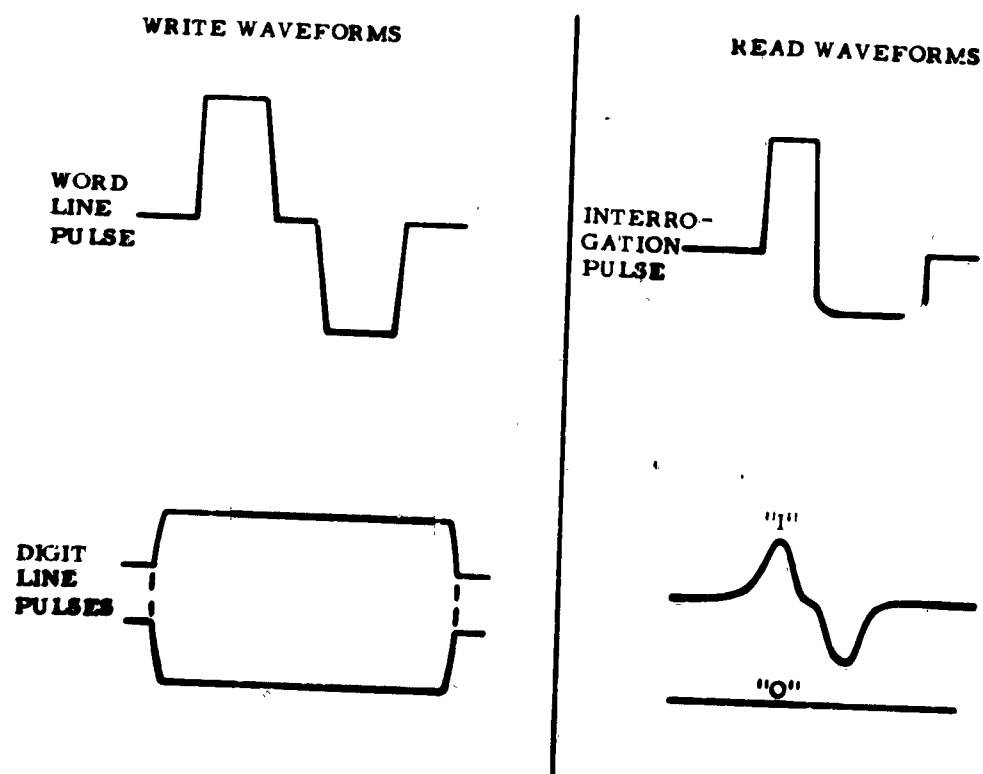
0.7 microsecond access time

50 watts power

7 × 7 × 7 cubic inches, memory stack volume

4 modules for memory circuits, each 6-1/2 × 6-3/4 × 1-3/8

Interestingly, the speed is slower than a typical state of the art MAD-NDRO. The speed performance figures quoted for the films are an order of magnitude less than inherent film speed. The major reason for this disparity is utilization of reduced drive currents and rise times than would be required for maximum speed. (Microelectronic drivers having 1 ampere drive at 20-40 nanoseconds rise are not available). At the reduced drive, film switching is primarily by wall motion as in conventional ferrite cores.



4833-22

Figure 2-29. Pulse Schedule

Volumetric comparison, judging by published data, is also disadvantageous to the film memory by a factor of least two to one. Current state of the art thin film memories employ word line densities on the order of 25 per inch. The problem of demagnetization due to fringing field phenomena is the chief barrier to higher densities. This is caused by the strip transmission line fringing fields as well as the demagnetization field of the film bit itself as it interacts with a neighboring bit.

4. Organization of Memory

Film memories are linear select organized to permit reasonable manufacturing tolerances in the individual spot characteristics. This results in an organization similar to Figure 2-20. A principle difference in circuitry is due to the low output level (of the order of 1 millivolt). A sophisticated sense amplifier design is required in order to discriminate against the common mode noise on the sense line of the ratio 1000/1 and the uncommon mode noise of 10/1.

BIAX NDRO Memory

Another NDRO memory is provided by BIAX, a ferrite element having the geometry shown in Figure 2-30. Recent reductions in the size of the BIAX element have increased its attractiveness for avionics memories. Additionally, a 2-wire array has been introduced which should have favorable impact on cost, size, and reliability. The new bix element has been termed the "Microbiac". Speed of operation as high as 10 mc/s has been demonstrated, but more typical speeds are in the range 1-2 mc/s.

1. Basic Operation of the BIAX Element

The operation of the BIAX element may be explained by reference to Figure 2-30. Information is stored in the element by setting the flux around the storage hole to saturation in one direction to store a zero or the other direction to store a one, just as is done in a toroidal memory. The flux around the interrogate hole is saturated in a fixed direction, independent of the data stored. The flux paths around the two holes interact in a common volume between the two holes. The resultant flux in the common volume is at an angle to the storage hole flux and interrogate hole flux as is shown in the vector diagram of Figure 2-30. Since the two flux paths interact in a very non-linear medium, increasing one will result in a decrease in the other and apparent rotation of the flux vector in the common volume as shown by the dotted lines in Figure 2-30.

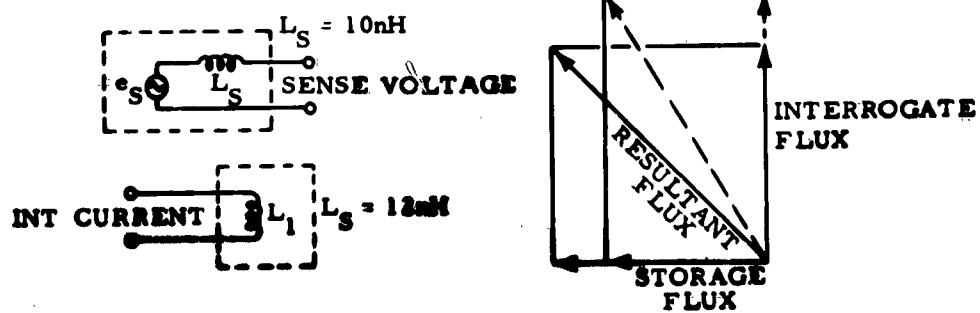
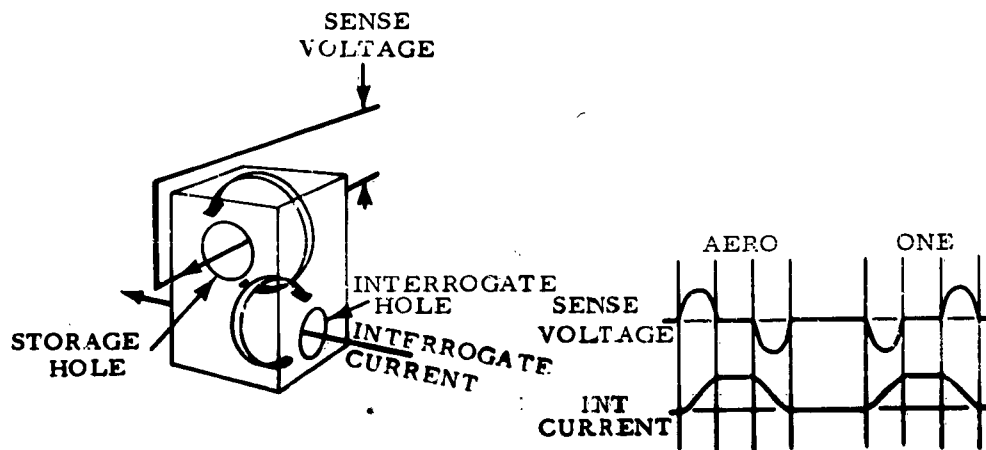


Figure 2-30. BIAx Principle

The application of a current through the interrogate hole in such a direction as to increase the flux around the hole will thus cause a decrease in the flux coupling the storage hole. This change in flux is sensed by a wire through the storage hole as shown. The polarity of the voltage induced in a sense line, as the interrogate current is applied, is dependent upon the direction of flux around the storage hole which represents the stored data. Thus the output signals for one and zeros are equal in magnitude, but opposite in polarity as shown in Figure 1-30b. Note also that a signal occurs at the termination of interrogate current and that the signal is of the opposite polarity to the at the application of current. This signal occurs as the flux around the storage hole and the interrogate hole return to the state that they occupied before interrogation. Since these changes are elastic no permanent change in the state of the element occurs as a result of interrogation. Thus, the readout operation is non-destructive.

2. Writing Techniques

As in other NDRO memories, writing is inherently low speed and is not normally used for real time operation. It is only performed when the program is to be loaded or altered. Two techniques have been devised, the standard write and the ratchet write.

3. Standard Write

This is accomplished by coincidence of word write and bit write pulses, see Figure 2-31. The word write consists of two pulses of opposite polarity, one of which adds to the bit current. Since the word current is twice the amplitude of the bit current, a 3:1 selection ratio is obtained. Note that the standard array requires 4 wires.

4. Ratchet Write

The coincidence of currents is achieved using current applied to both the storage hole and the interrogate hole, see Figure 2-32. This allows a two wire system. Waveforms of the write currents are shown in the figure; the polarity of the bit current determines whether a "one" or "zero" is written. Note that at least two pulse pairs of the word current are required.

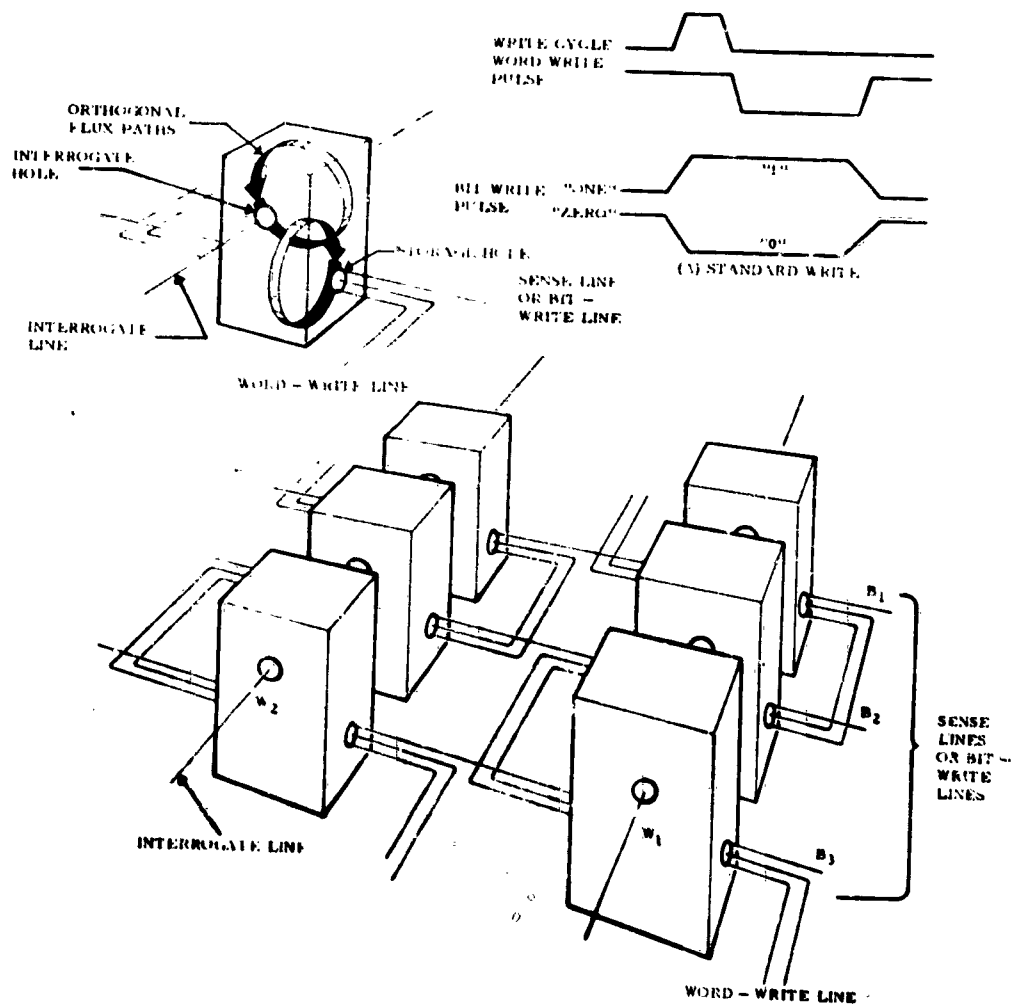


Figure 2-31. Standard Write

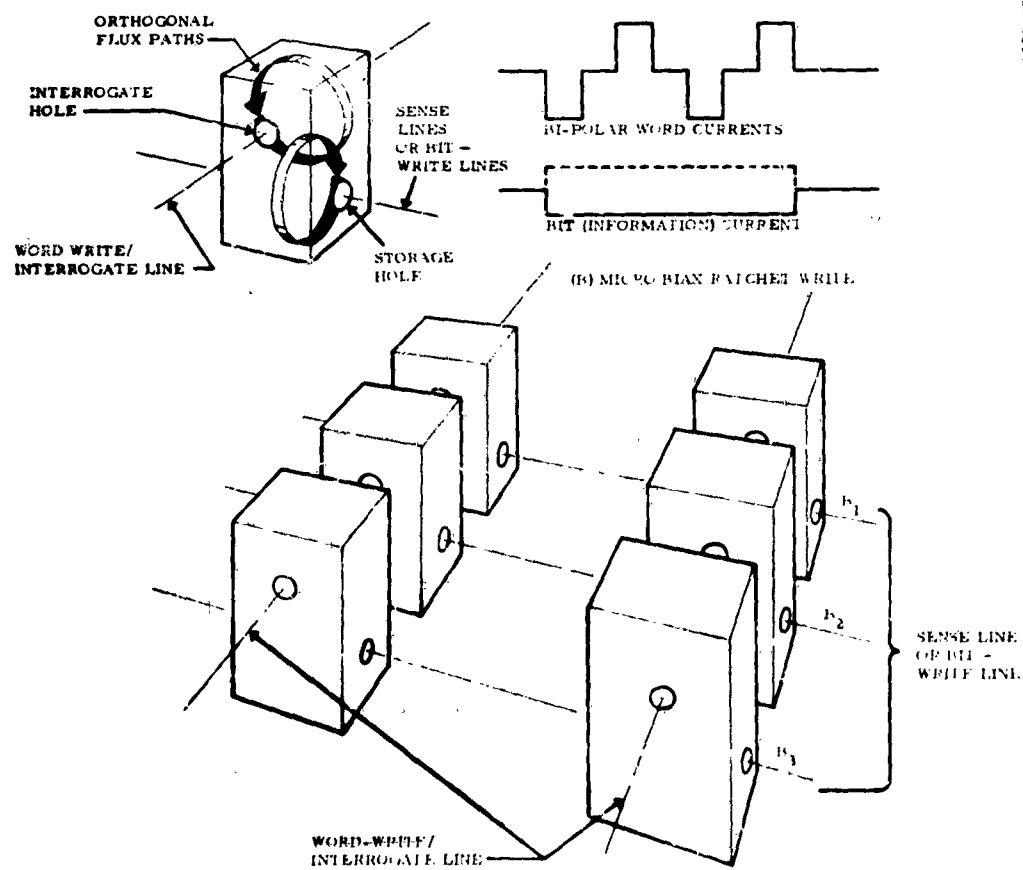


Figure 2-32. Micro-BLAX Ratchet Write

The last pulse is in the direction of the interrogate current pulse so that the flux in the interrogate hole is left in an direction that will be reinforced by the interrogate current. The amplitude of the bit current is such that it is not sufficient to significantly disturb the stored flux in the absence of word write pulses.

5. Comparison of BLAX and Microbiac Elements

Table I-5 shows the characteristics of the type "03" micorbiac and the type "06" standard bias manufactured by Raytheon. Both are intended for wide temperature operation as found in an avionics application.

Temperature variation of the word and bit writing currents and interrogate currents is used to maximize the output signal, see Figure 2-33. Of course, with respect to the write currents, this can only be done if the operating temperature is fixed and known beforehand. However, wide tolerance in writing current is permissable on the order of ± 30 percent, see Figures 2-34, 2-35 and 2-36.

Array Size and Organization

1. Array Characteristics

The microbiac array is fabricated with elements on 0.034 centers in both word and bit directions. The resultant density is competitive with other NDRO memories. The memory is 1" near select organized. Output signal level is 4-5 millivolts, which is intermediate between MAD and film. A sophisticated sense amplifier and strobe system is required to discriminate against common mode noise inherent in sharing of the sense line conductor for write and read function in a two wire array.

DRO Core Memory

1. Introduction

For DRO, both two cores per bit with linear selection and single core, coincident select organization have been used. Wide temperature operation to 125°C has been achieved in both types with lithium ferries and the

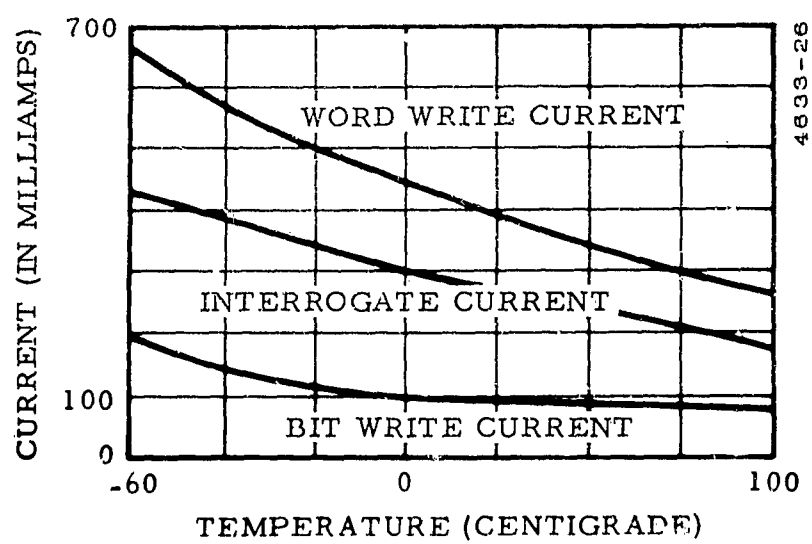


Figure 2-33. Temperature vs Current

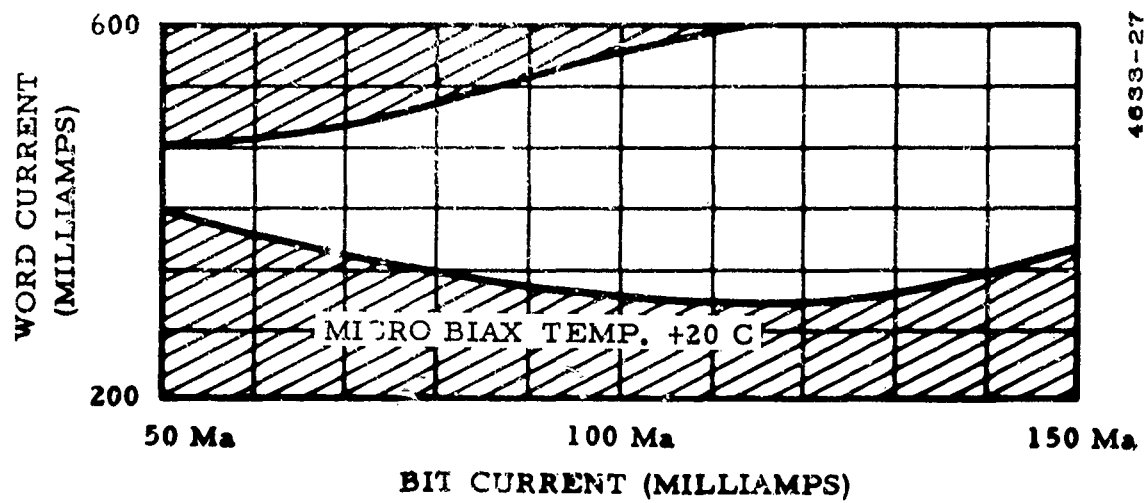


Figure 2-34. Micro-BIAX (Temp +20C)

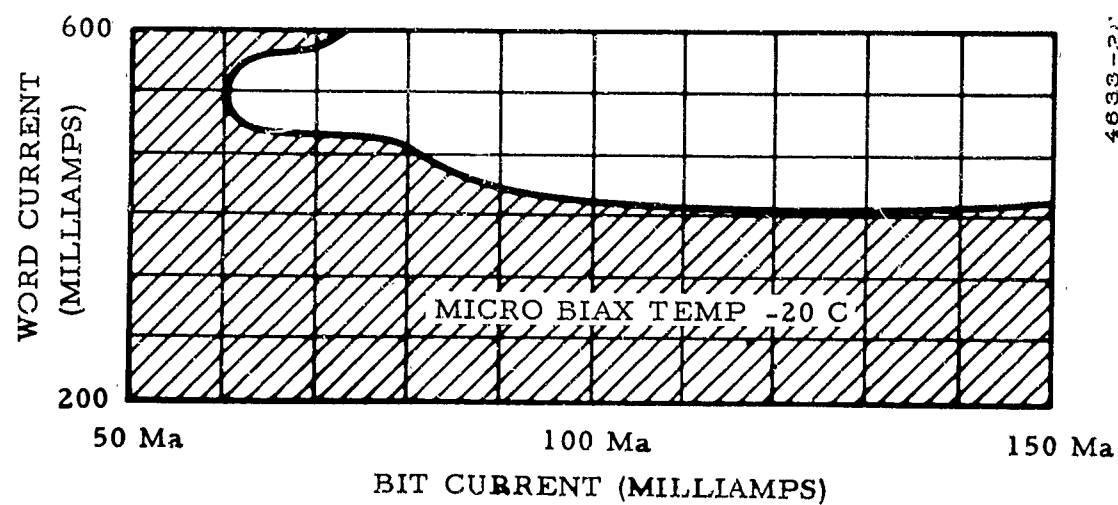


Figure 2-35. Micro-BIAX (Temp -20C)

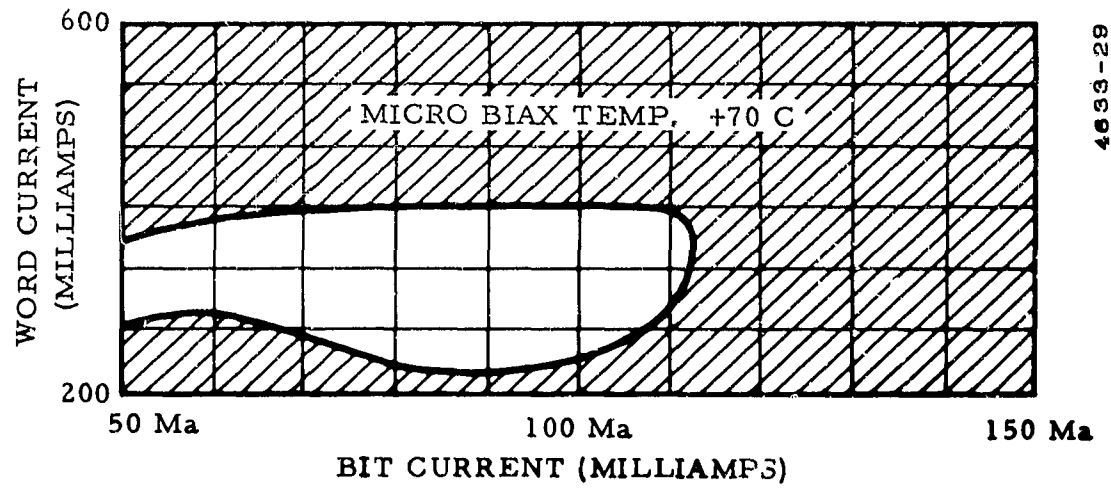


Figure 2-36. Micro-BIAX (Temp +70C)

use of tracking power supplies (required in single core organization only). Volumetric efficiency and power of the single core memory is favored by a factor of two over the two core per bit. Cycle time, however, favors the latter by the same factor. Thus clear cut tradeoffs in terms of power, speed, and size may be made.

The DRO memory to be described consists of a basic module of 4096 words of 24 bits each. The memory module is organized for coincident-current operation as shown in Figure 2-37. Access time for the memory is 440 nanoseconds. Total read-write cycle time is 1.88 microseconds. The design provides operation over the full temperature range encountered in the avionic environment. Figure 2-38 shows a typical 4096-word module

2. Memory Stack

The memory stack uses 22-mil lithium cores wound in 4096-core arrays. Four wires thread each core; an X wire, Y wire, inhibit wire, and a sense wire. One 4096 core array is used for each bit in the word. Four of the 4096 arrays are fabricated on one plane and six of these planes make up the stack.

The complete stack occupies a volume of $3\text{-}7/8 \times 3\text{-}7/8 \times 1\text{-}1/4$ cubic inches. The diode matrices which provide selection to the X and Y lines are located below the stack.

3. Circuits

The circuits associated with the memory matrix are:

Timing and control circuits

Address register and logic

Address selection drivers

Inhibit drivers

Sense amplifiers

C-Register and logic (input-output register)

The drivers and selection circuits are fabricated from thin-film hybrid circuits using hermetically sealed silicon components for active devices. The logic gates, control circuits, and sense amplifiers are monolithic integrated devices.

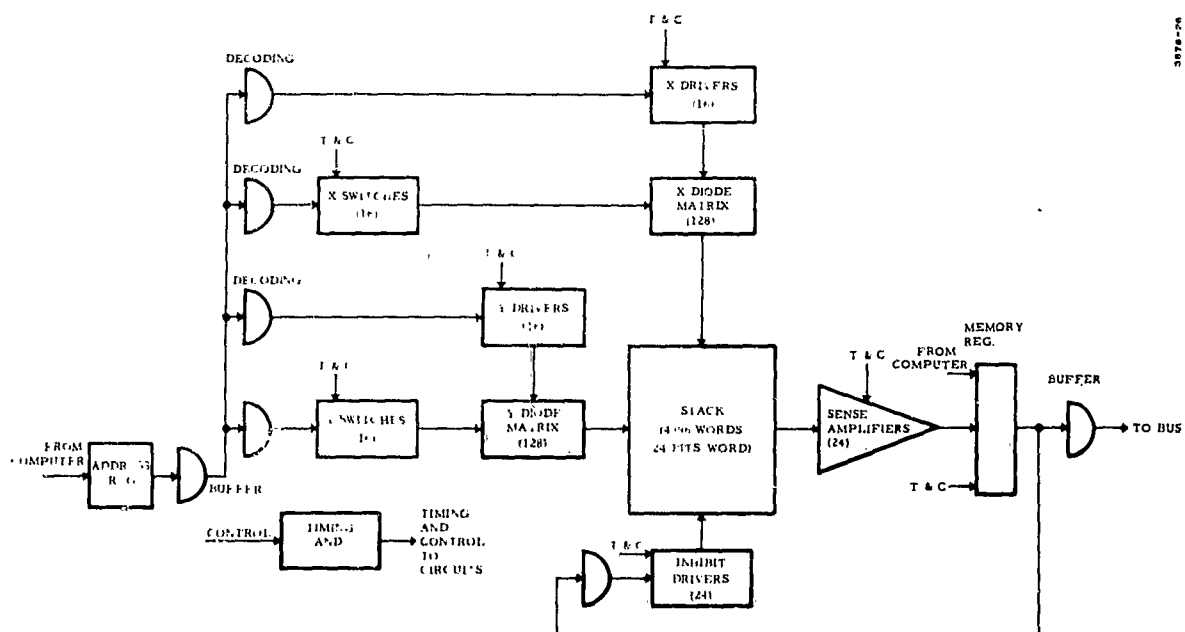
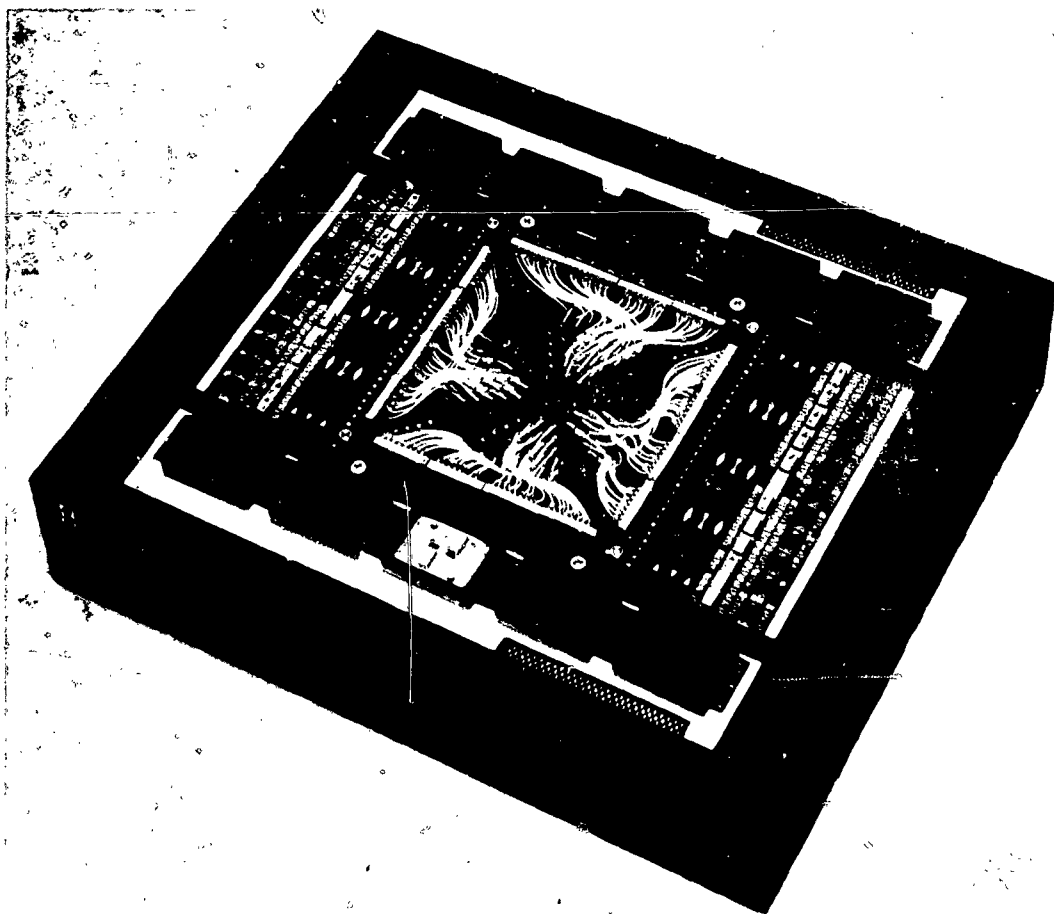


Figure 2-37. DRO Block Diagram



9876-75

Figure 2-38. DRO Memory Module

4. Current Drivers

Two basic circuit configurations are used for the current drivers; one is designated a driver, the other a switch. X or Y currents are derived from a driver-switch pair. An inhibit driver is simply one of the drivers.

- a. Driver, Coincident Memory — The driver circuit serves as a series switch from a current source to drive word lines in conjunction with the switch circuit, or to drive digit lines. As shown in Figure 2-39, the driver switches current into the load as a function of logic timing pulses where a true/open level input maintains the switch (Q3) open; a false level (0-volt nominal) closes the switch.
- b. Switch, Coincident Memory — The switch circuit functions as a series switch in the memory word line. As shown in Figure 2-40, it opens and closes as a function of logic timing pulses where a true/open level maintains Q2 open, and a false level closes the switch. The switch sinks current to V_{BB} and current compensation is achieved as a function of a change in V_{BB} . The first stage of the switch circuit is designed to furnish a constant current input to the base of Q2 independent of the change in V_{BB} required for compensation. The turn-on time delay is typically on the order of 50 nanoseconds, the turn-off time on the order of 75 nanoseconds. The rise and fall time is on the order of 100 nanoseconds.

5. Sense Amplifier

The sense amplifier accepts input signals from a memory sense line, determines whether the signals represent a logical "one" or "zero" and generates output signals which are compatible with computer logic circuits. To accomplish this, the amplifier amplifies the small differential mode signals, which contain the memory information, rejects common mode signals, establishes a threshold for discrimination of the input signal amplitude, and generates an output whose amplitude and duration are independent of the input. The amplifier must be capable of rapid recovery from overload, and maintains stable operation over extremes of temperature and repetition rate.

The sense amplifier contains: a line or differential amplifier, an OR gate which accepts signals of either polarity, a threshold detector, an AND gate for time coincidence with a strobe pulse, and a "one shot". A schematic diagram of the circuit is shown in Figure 2-41.

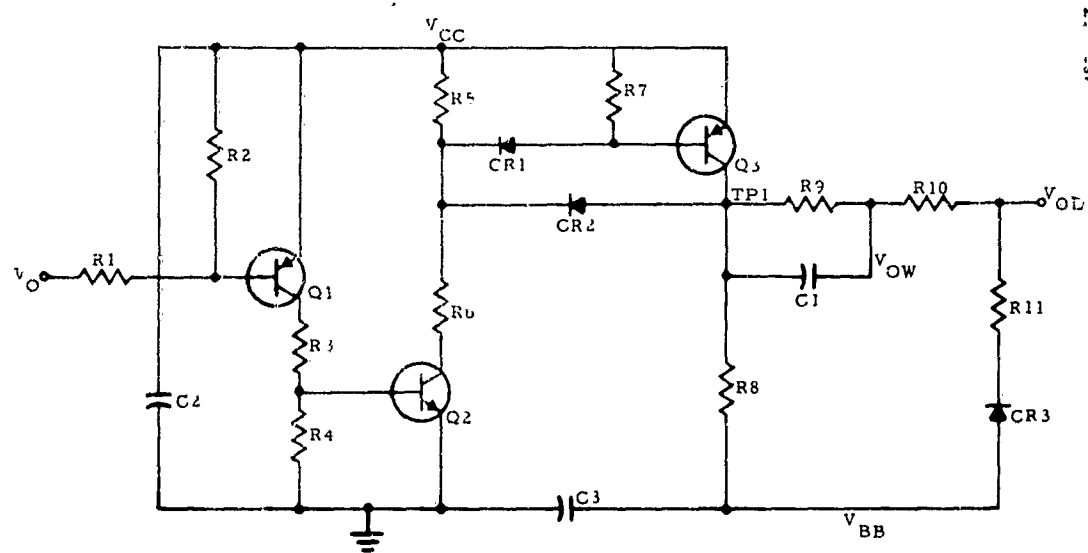
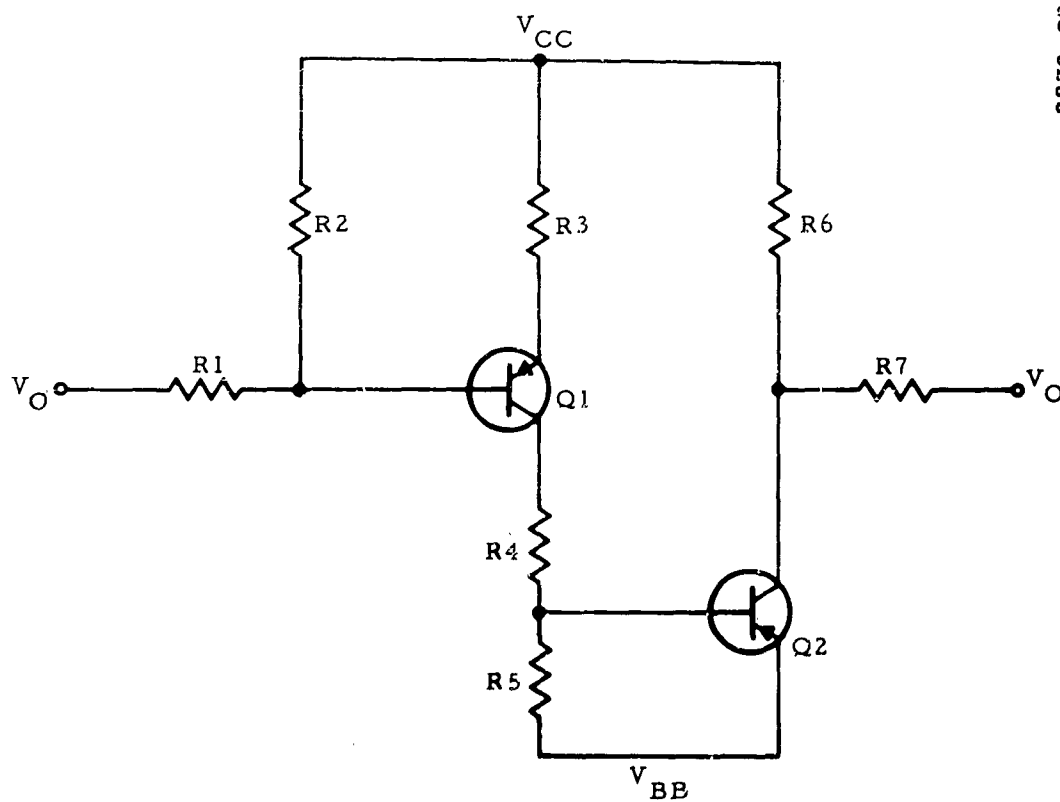


Figure 2-39. DRO Driver Schematic



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Figure 2-40. DRO Switch Schematic

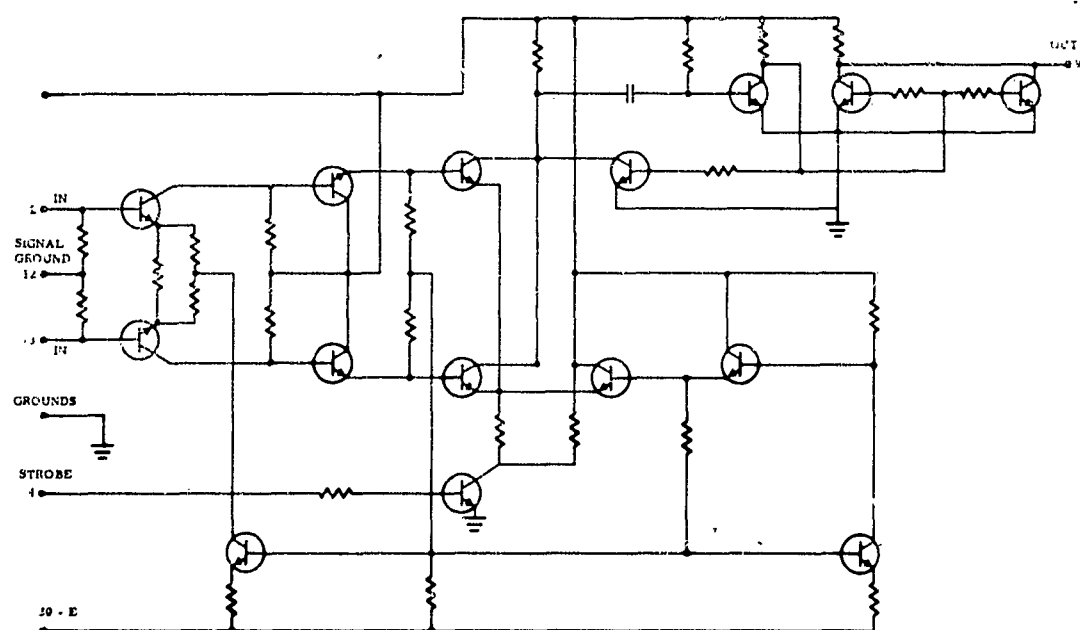


Figure 2-41. DRO Sense Amplifier

6. Logic and Selection

The address register has the outputs of each stage and their complements available. Additional gates are provided for fan-out buffers, as shown in Figure 2-42. The outputs from the buffers are decoded into 8 by 8 selection matrices, one for X-selection and one for Y-selection. Since bipolar currents are required in each drive line, a driver-switch pair is actually required at each of the 8 by 8 positions, and two diodes are required for each drive line. To select any given drive line, a drive-switch pair corresponding to that line is selected simultaneously during the READ cycle. During the WRITE cycle, the other drive-switch pair corresponding to that line is simultaneously selected, causing current to flow in the opposite direction through the same line. At the same time that a set of X-drivers is selected, a set of Y-drivers must also be selected to permit the coincidence of the two currents to select a given word in the stack.

7. Timing and Control

The timing and control circuits generate all timing signals used for memory operation. In the memory under discussion they are organized into two sections, as shown in the block diagrams of Figures 2-43 and 2-44. One is for control of the READ operation; the other is for control of the WRITE operation. The operation of each section is initiated independently by the computer by a command pulse. Upon receipt of the command pulse, the read timing section generates the following signals:

- a. Read-Switch Time -- Routed to all read switch selection gates to determine the on-time
- b. Read-Driver Time -- Determines the read drive "on" time; it is contained within the read switch time
- c. Strobe Time -- Routed to all sense amplifiers to provide time coincidence with the memory output

When a write command signal is received, the following signals are produced:

- a. Write-switch time
- b. Write-driver time

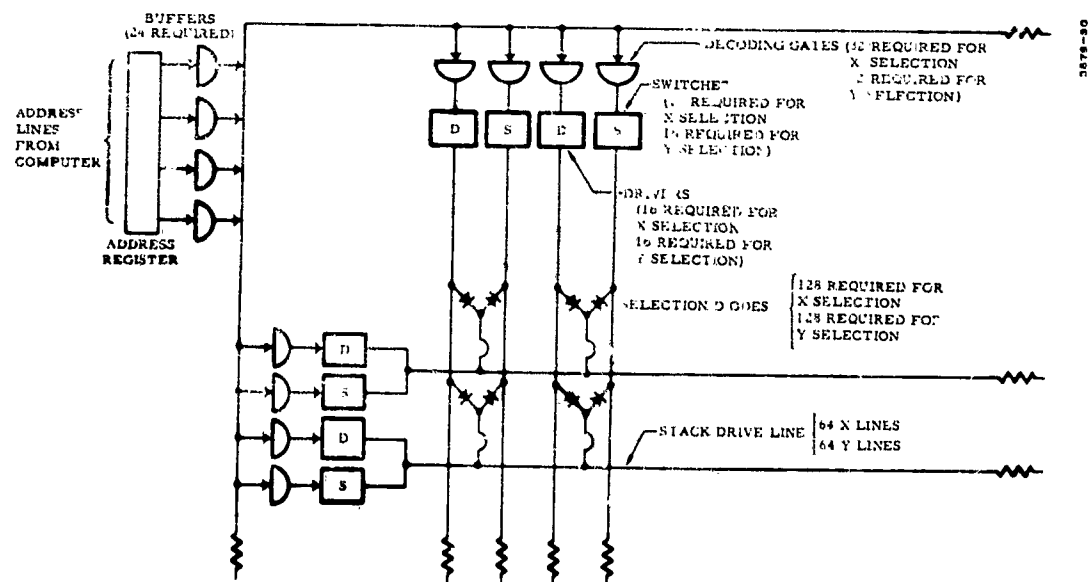
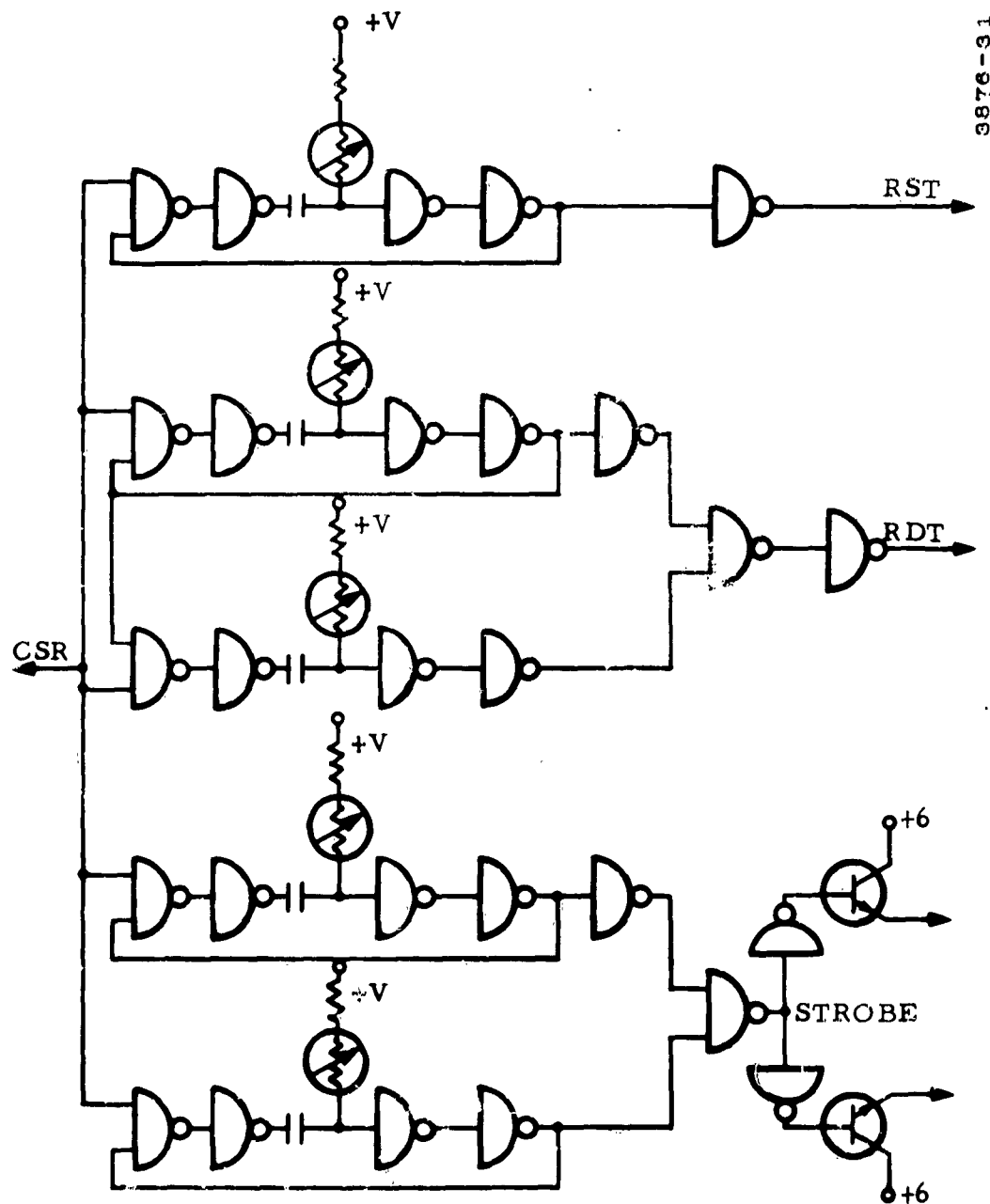


Figure 2-42. DRO Selection



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Figure 2-43. DRO Read Timing Block Diagram

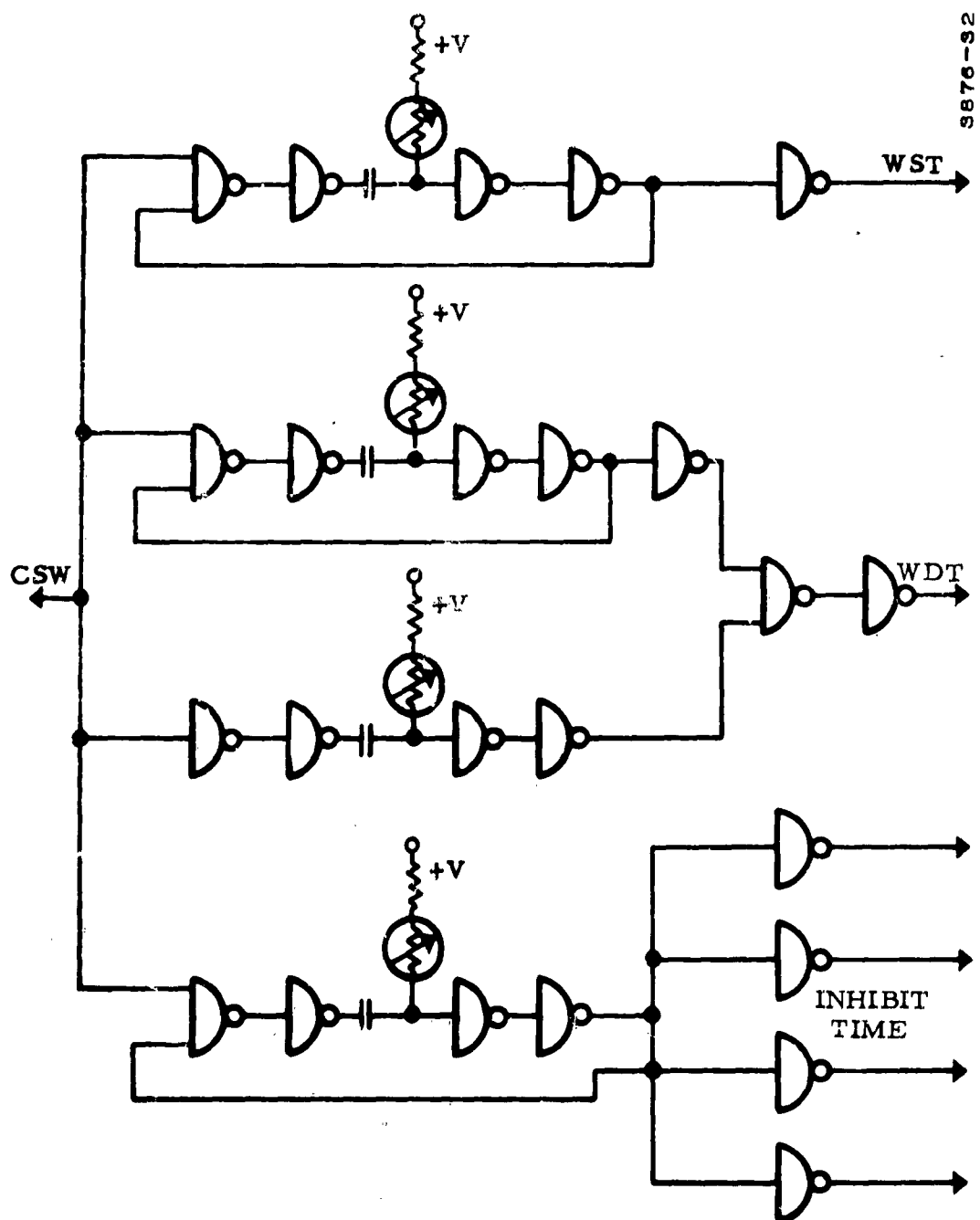


Figure 2-44. DRO Write Timing Block Diagram

- c. Inhibit time-transmitted to all inhibit drivers to establish the inhibit current timing. All other times are contained within the inhibit time.

The timing relationships for this memory are shown in the timing diagrams in Figure 2-45.

8. Power Requirements

The power dissipation of the 4K DRO is 12 watts in the standby or non-interrogate state and increases to 70 watts in the operate or interrogate state. A variable voltage regulator utilizes a temperature sensor in the core stack to provide a variable output for the current sources. Temperature tracking is obtained from -55°C to $+125^{\circ}\text{C}$.

Thin-Film DRO

DRO thin-film memories meeting aerospace environment requirements are available. These memories are fabricated of permalloy ($\text{Ni} - \text{Fe}$) and typically are on the order of 2000 Å thick with individual bit size of 30 mils \times 30 mils. Thickness of the element determines the signal output and thus a lower limit in this area is set by signal to noise considerations. Area of the individual bit is determined by the same considerations as were discussed under NDRO thin films. A state of the art stack design incorporates 139,264 bits (or 5820 words of 24 bits each) in a volume $4.2 \times 4.2 \times 4.2$ cubic inches (.04 cubic feet). The stack also contains the selection circuits comprised of micro-diodes and tape-wound cores.

DRO film memories have been produced for commercial application with cycle times as low as 32° nanoseconds. Additionally they have been demonstrated in the laboratory with cycle times as low as 100 nanoseconds. However, for the same reasons as previously cited for NDRO, DRO memories produced for aerospace application have cycle times on the order of 4 microseconds. This constitutes a serious limitation on their use for avionics purposes.

Wired Memory

Another form of NDRO memory may be constructed using an array of ferrite cores. Consider initially that such an array has all ONE's

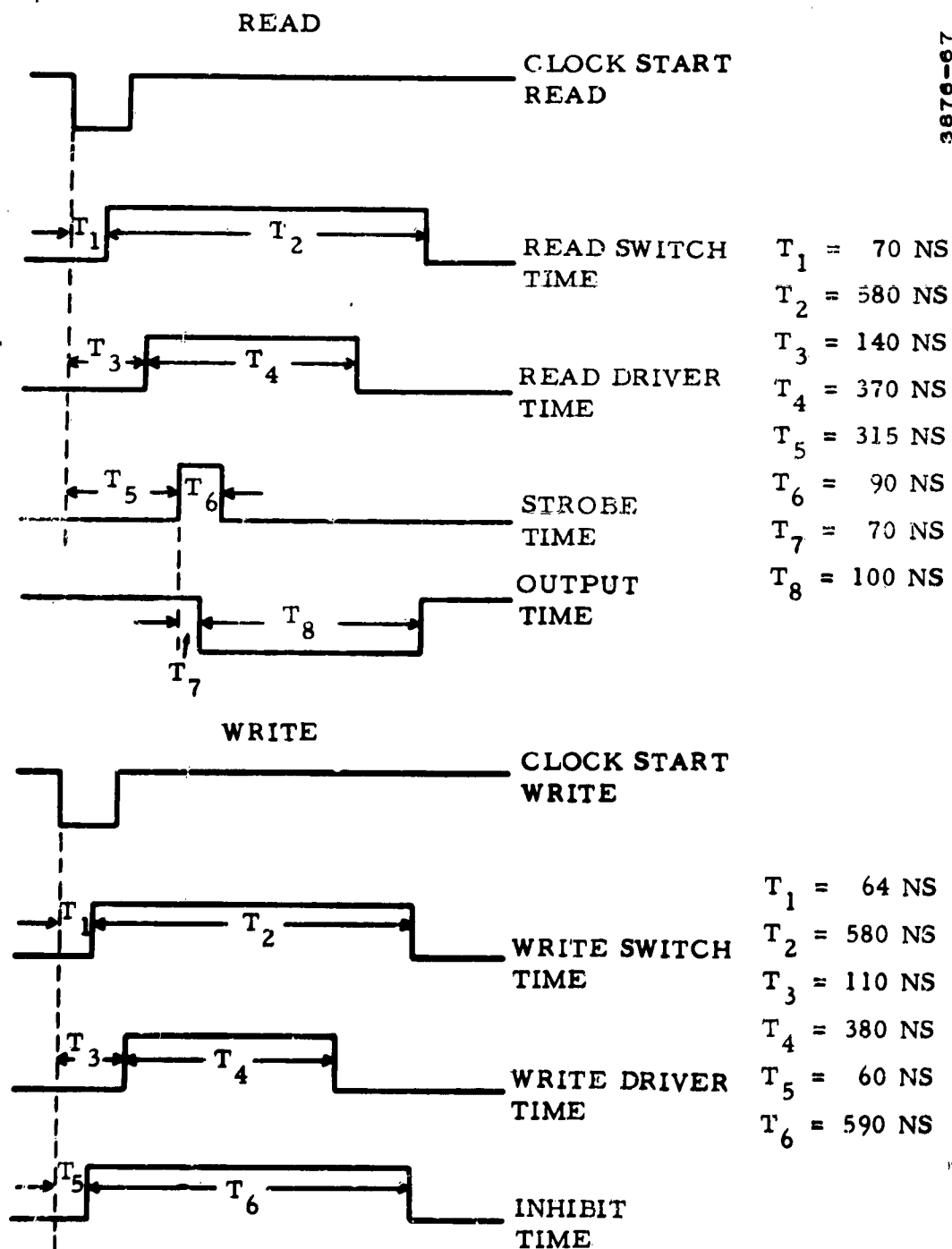


Figure 2-45. DRO Timing Diagram

written into it. This may be accomplished, for example, by the simple expedient of energizing a reset winding linking all the cores of the array. A zero can be inserted into any core position by any of the following techniques:

- a. Omitting the core
- b. Removing the core
- c. Shorting the core with a single turn winding
- d. By passing the core with the sense or drive winding

Wired memories use method 4 which in effect stores the data in the wiring configuration rather than the core. This has the outstanding advantage of being able to achieve high storage density through the expedient of running a multiplicity of wires through each core.

Wired memories, once constructed, cannot have their information electrically altered. Any change in the information content requires either a new memory or physical alteration (usually unfeasible). This is in contrast to other NDRO types such as MAD and the thin film bicore where the contents can be completely changed, though not usually in real time. Wired memories should only be applied, therefore, to fixed program and constant storage that have been thoroughly checked out.

1. Organization of Wired Memories

Wired memories have been organized and constructed in the following configurations:

- a. Linear select, with storage in sense or drive lines
- b. Direct selection, storage in sense lines
- c. Coincident current select, storage in sense or drive lines.

The linear select wired memory has been implemented using tape-wound permalloy cores rather than the conventional ferrites. This is possible because the cores are used as energy transmitters in lieu of their normal role as storage and switching devices. However, this slight advantage is negated by the complex address selection and decoding required in word organized systems.

Direct selection is implemented by so-called CORE ROPE memories. Because of its extremely efficient address selection technique, core rope has been very widely applied to small memories (several thousand words maximum). For such applications, core rope provides an NDRO system at a cost of 25% of an equivalent MAD-NDRO, for example. The simpler circuit configuration also has the merit of higher reliability. These characteristics have led to wide usage of core rope in space applications such as the Apollo spacecraft.

For large memories, the basic core rope has the disadvantage of large power dissipation and large cumulative noise from unswitched cores. Coincident current organized wired arrays retain address selection simplicity and permit exploitation of simple noise cancellation techniques to achieve good signal to noise ratios.

2. Organization of Coincident Current Wired Array

The basic memory organization is that of a "wired" coincident current memory resulting in a permanent NDRO storage. With this wired memory technique, 192 cores store 12,288 bits of information. Random access is provided for all memory locations. Figure 2-46 is a block diagram of a 512-word core rope memory. Word readout is in parallel with information available approximately 0.8 μ s after the start of a read pulse. The complete Read-Reset cycle time is 2 microseconds.

3. Storage Device

Wired coincident current memories may advantageously employ tape-wound cores. A desirable feature of a tape-wound core as a memory device is the comparatively low switching current necessary to toggle the core in a binary mode as compared to a ferrite device. The tape-wound core possesses a more stable temperature coefficient than a conventional ferrite device, eliminating the need of an elaborate temperature-dependent current source and its associated thermal sensory units. Thus, the memory can be designed to operate over the temperature range from -55°C to 125°C with ± 10 percent variation in supply voltages. One slight disadvantage is that a sharp switching threshold is not as pronounced in a tape-wound core compared to a ferrite device. Additionally, the tape-wound core is more costly, though this consideration is minor since one core stores 64 bits.

A suitable tape core for this memory has the following characteristics: material = Permalloy 80; flux capacity = 30 maxwells; ID = 100 mil; OD = 220 mil; height = 100 mil.

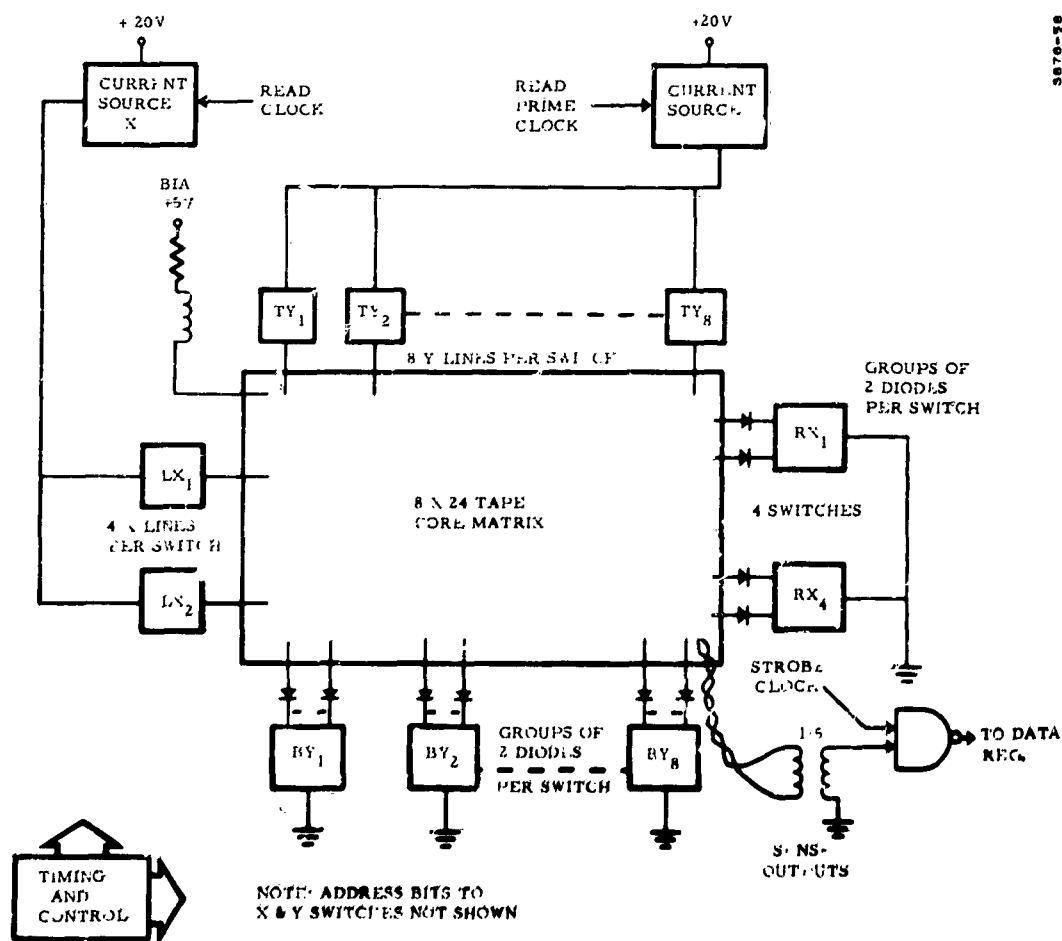


Figure 2-46. Block Diagram of a 512-Word Core-Rope Memory

4. Selection Technique

The system is a random-access memory. Word selection is by a coincidence of an X-Y current. End-fire techniques on both X and Y axes are used to advantage to minimize the number of selection switches.

There is no reset circuitry associated with this memory except in the form of a simple bias winding which links all the cores in the array. This method automatically resets the cores and eliminates the need of retaining the word address during this phase of the memory cycle.

Separate pulsed current sources are provided for the X groups of selection lines and the Y-group of selection lines. The line switches themselves are operated in the saturated mode to minimize the power dissipation of the device.

5. Sense Circuits

Because the core outputs are relatively high, on the order of 200 to 300 millivolts, there is no need for a sense amplifier. A simple step-up transformer is all that is required to bring the core output to a usable level for directly gating or setting a register. Any threshold level adjustment usually found in most sense amplifier circuits is eliminated. However, a time discriminating pulse is used in much the same manner as in most memory systems.

6. Winding Configuration

The wiring of the core array is of simple design. 64 "Y-lines" (word lines) are wound continuously through each core intended to store a "one." Another set of 8 "X-lines" subdivides the cores into groups of 24 cores which is the word length. One can therefore visualize a rope of 64 wires essentially "snaking through" the cores. The bias or reset winding threading all cores increases the number of wires in this rope from 64 to 65. Figure 2-47 depicts the wiring for the 512 word, 24 bits/word memory.

A 2-turn sense winding links similar bit positions of the 8 groups of 24 cores. Due to very low disturbances during readout, a noise-cancelling scheme is not necessary in the sense lines, resulting in a simple core array design.

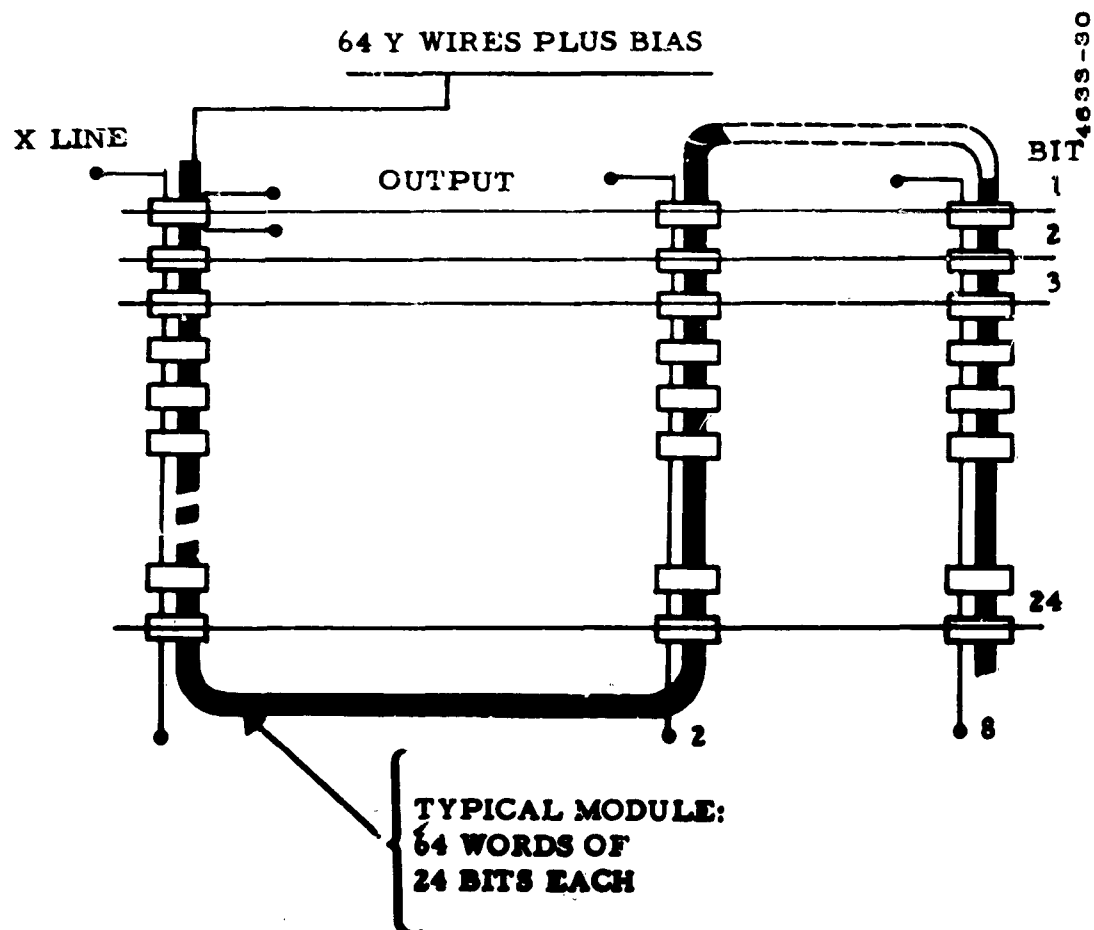


Figure 2-47. Winding Arrangements

2.2.4 Multi-Track Airborne Tape Unit

In order to provide an airborne computer system with additional capability and flexibility, a multi-channel airborne tape unit may be used. The primary uses of an airborne tape unit in conjunction with avionic computers are as follows:

Provides for storage of operational or mode programs in NDRO form. Programs may be dumped into computer DRO memory when called upon at rates up to 88,960 bits per second or 8192 words of 24 bits of data or instructions in approximately 3 seconds.

Provides for storage, off-line but with rapid access, of built-in test programs both for computer system test as well as test of other avionics systems and subsystems.

50-million bit capacity provides storage for data recording for flight test programs as well as in-flight data monitoring.

Other principal features of a multi-track airborne tape recorder are listed below:

1. Packing Density: up to 55 bits per inch
2. Tape Length: up to 1000 feet
3. Number of Tracks: 9
4. Tape Width: 1/2 inch
5. Tape Thickness: 1 mil
6. Tape Speed: 20 inches per second
7. Data Transfer Rate: 90,000 bits per second, maximum
8. Rewind Speed: 100 inches per second (average)
9. Start Distance: 1 inch
10. Stop Distance: 1.5 inches

11. Transport Size: 10" X 9" X 6" (typical)

12. Transport Weight: 15 pounds

13. Transport Power: 71 watts

2.2.5 Future State of the Art

Introduction

A major trend in memory research and development is in batch fabricated systems. Effort is being exerted primarily for the commercial market and its more modest environmental requisites. Examples recently reported in the literature include the wafile iron memory (1963), flux memory (1964), semiconductor memory (1964), together with new improvements in ferrite technology.

The major interest in batch fabricated memories stems from the desire to improve cost and density factors. The reduction of cost appears plausible due to the higher degree of automation inherent in batch processing. However, a high degree of automation has been achieved in the fabrication of discrete core planes such that costs range today between two to five cents per bit for wired arrays. Further complicating the cost picture is the fact that selection of individual components is automatically performed. This places batch technology at a disadvantage until very high processing yields are realized. Individual selection also often permits cheaper addressing (coincident current versus word select) and wider operating margins in associated memory circuitry. Factors such as these have limited, to this time, the employment of thin films and ferrite aperture plates - though both were introduced more than five years ago.

Though discrete memories have achieved very respectable densities (400 elements per square inch), greater densities are desired. At such density, a 4096 word, 30 bits/word memory requires approximately 400 square inches of plane area. In comparison, a 1/4 X 1/4 inch micro-circuit has the potential for containing up to 1000 transistors. Such density is beyond the capability of present known magnetic batch memories.

Efforts to improve both the cost and density factors through new memory designs or material will now be described.

Waffle-Iron Memory

This memory has been described as having: (1) low cycle time (200-400 n seconds); (2) low cost per bit; (3) reliable performance over wide temperature range; and (4) useful for DRO and NDRO.

The waffle-iron structure consists of a soft, high μ ferrite base plate and a thin, plated overlay of isotropic nickel-iron alloy. This is shown in Figure 2-48. Slots are milled into the ferrite base on 15 mil centers in both the word and digit directions. Word and digit lines are then laid in the slots. The overlaid nickel-iron thin film (on a copper substrate) provides the storage, while the ferrite provides a closed path for the flux. The closed path feature makes the waffle iron less sensitive to disturbing fields than is a conventional thin film memory. From the manufacturing point of view, the device is open loop leading to ease of fabrication and assembly.

Word-organization is employed in the waffle iron. Typical driving currents are 400 mv for the word drive, 150 for the digit drive, with an output of 10 mv during read operations. In experimental memories of 256 words low back emf and short propagation times (4-9 nsec) were experienced, giving encouragement that large arrays would be practical.

Flute Memory

This batch memory derives its name from the fact that its geometry is that of a number of parallel tubes (resembling flutes), intersected by an orthogonal set of bit lines. The geometry of the flute memory element is shown in Figure 2-49 and a cross-sectional view with dimensions shown in Figure 2-50. The flute structure was selected on the basis of its suitability for a high degree of automatic fabrication.

Flute memory planes are fabricated by die molding bit and word structures with matched grooves. The grooves are filled with a mixture of ferrite in a resin binder in which are sandwiched the grid structure representing the word and bit lines. After assembly of the structure, curing, heat cycling, and sintering processes are used to achieve the desired hysteresis loop characteristics.

Experimental flute memory planes have been produced with 33 word lines per inch and 50 bit lines per inch. Flute diameter in these planes has been 0.005 inch. Operating in the bi-polar word-bit mode with

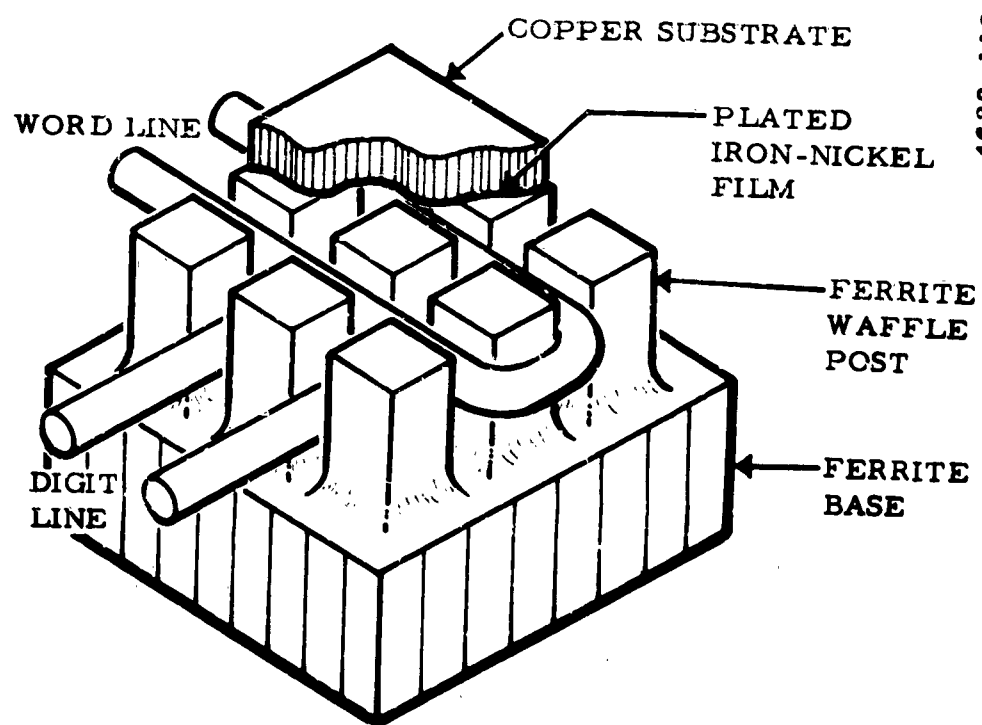


Figure 2-48. Waffle-Iron Structure

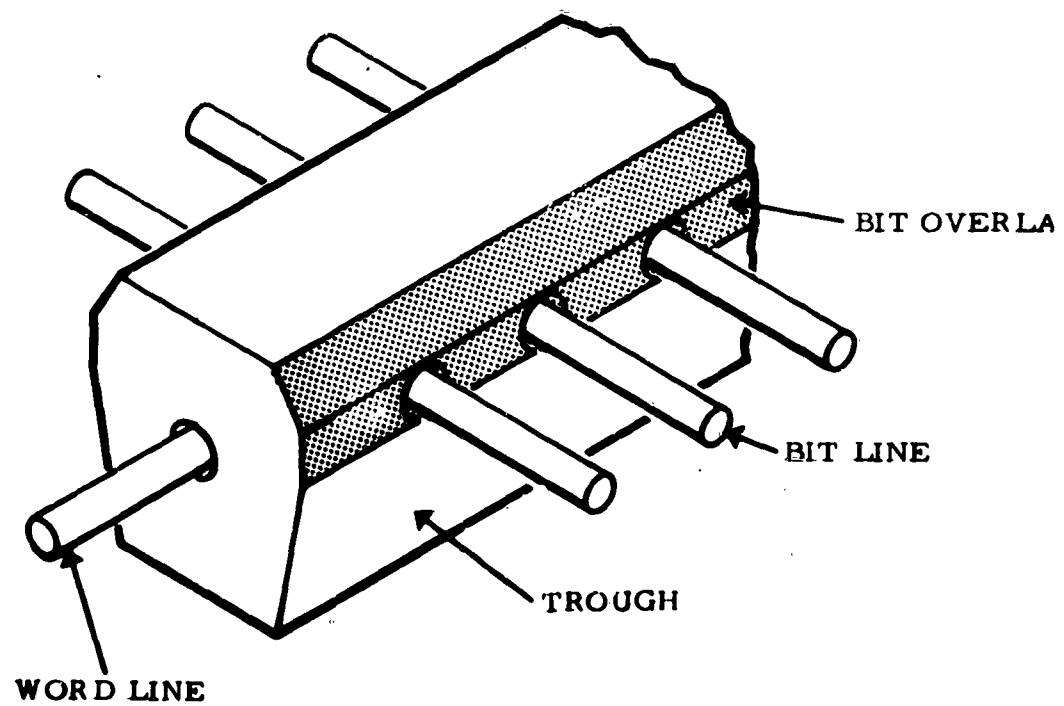


Figure 2-49. General Configuration of the Flute Memory Element

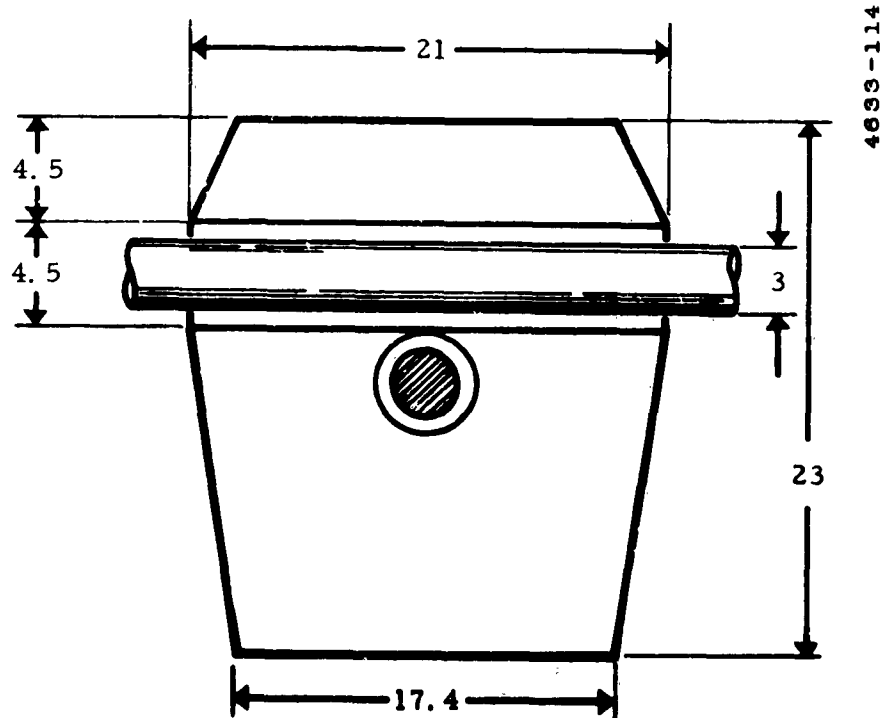


Figure 2-50. Cross-Sectional View of Flute Memory Element

currents of the order of 100 mv, the output signals are of the order of 5 mv. Cycle times under 1 microsecond have been achieved. Projections are for 250 nanosecond read time at 800 ma read drive and densities of 10^4 bits/in.² to be achieved.

Laminated Ferrite Memory

This type of memory consists of a monolithic sheet of ferrite with embedded conductors and is made by the lamination of ferrites. Three ferrite sheets are used to form the laminate. The top and bottom sheets, of thickness 2.5 mils, each contain a winding set consisting of parallel conductors. Spacing of the conductors is at 10 mil intervals. Top and bottom windings are orthogonally related, forming the typical x-y grid used in ordinary memories. The top and bottom sheets are separated by a center ferrite sheet of 0.5 mils thickness. Thus, overall thickness of the three sheet laminate is on the order of 5.5 mils. Sheet areas as large as 16" X 16" have been fabricated. However, a more common size is 1" X 1" which contains 32 words of 32 bits each.

Individual memory elements in the monolithic array are formed, in effect, at the crossovers of the x and y windings. The equivalent size of these elements is on the order of 2-3 mils. With an effective conductor spacing of 10 mils, it is seen that the equivalent memory cells in the monolithic sheet are essentially isolated.

1. Performance Characteristics

For memory cycle times on the order of 1 microsecond, the following currents are required in DRO operation:

1. write - 150 ma
2. read - 400 ma
3. digit - 30 ma

At these currents, the sense signal is approximately 30 millivolts. Sample planes tested at Litton confirm these data. The sense signal remains fairly constant over a wide range of temperatures.

Cycle times as low as 100 nanoseconds have been claimed in the literature. However, correspondingly low sense voltages are obtained - 1 to 2 millivolts.

2. Operating Mode

The memory is operated in a word organized mode. All bits of a selected word receive the same read-write current in this mode. A two bit per memory element configuration is used, i. e. , two cross-overs per bit. This operating mode provides excellent signal to noise ratio even at high operating speeds. (High speed operation of ferrite memories reduces the signal component due to achieving only partial switching and increases the reversible magnetization component which represents the noise.)

An optimum digitizing scheme with two crossovers per bit is to apply write current to the word line (x-winding) and simultaneously digit current to the appropriate bit windings (y). The selection of the y winding to be driven is dependent on whether a "1" or "0" is to be written. During the read, word line current is applied in opposite direction to the write current. Depending on whether a "1" or "0" has been written, one of two different polarities of voltage is generated on the pair of y windings, which now function as the sense windings. The voltage is differentially sensed at the output of the y windings.

3. Fabrication Techniques

Three operations are used in the fabrication of the laminated ferrite memory. These are: "Doctor Blading;" "Laminating and Sintering;" and "Conductor Screening."

Doctor Blading: In this operation the green ferrite sheets are prepared. The method consists of spreading an even layer of ferrite mixed with organic binders on a glass plate. The tool used for spreading the mixture is similar to a doctor's scalpel, hence the name. After air drying occurs, the ferrite sheet is peeled off the glass surface.

Lamination: The three sheets comprising the memory are laminated together using an hydraulic press. Only moderate pressures and temperatures are required. The result of this operation is a uniform isotropic material with no trace of delamination marks.

Conductor Screening: To form the conductors on the "green" ferrite sheets, a process similar to silk screening is used. A mask of the conductor pattern is placed in a glass substrate. Conducting paste is squeezed

on the glass through the mask. The mask is then removed and ferrite is doctor bladed into the pattern and glass substrate. The ferrite sheet with embedded conductor pattern is peeled off after air drying.

Advantages of low drive current requirement, high speed and small element size were previously discussed. Element size of 2-3 mils is the smallest of any known technique. High signal output at low drive implies simple memory electronics as well as reasonable noise tolerance. Finally simplicity of the manufacturing technique, without time consuming setup times, should be translated in low cost per bit. These characteristics, if proven in production, could well eclipse many competitive techniques.

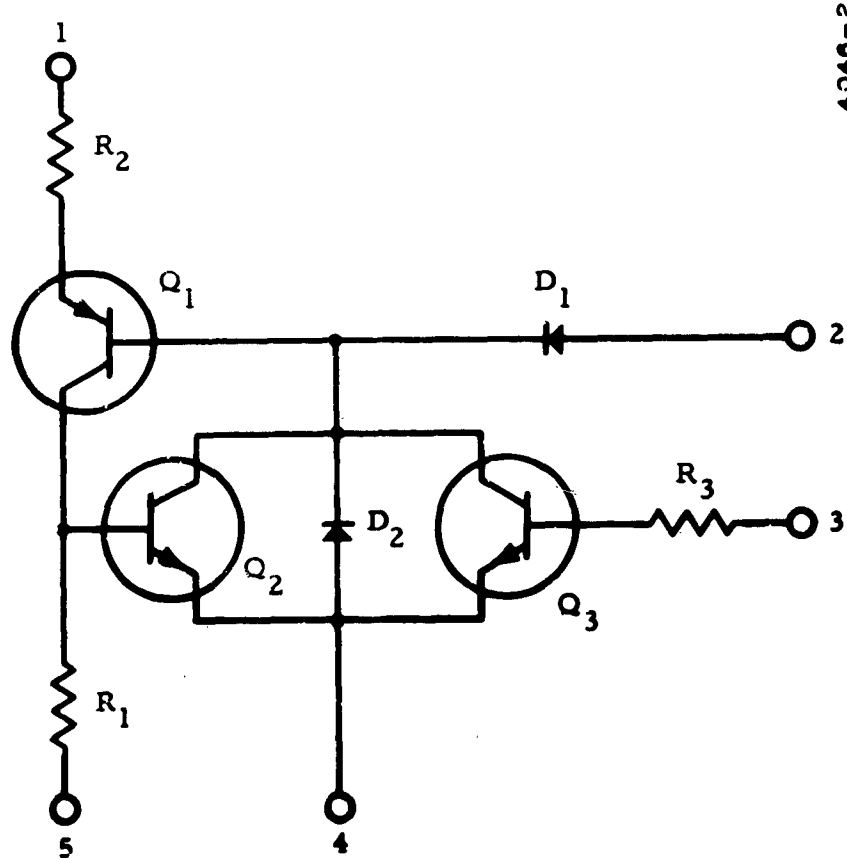
Semiconductor Memory

A novel semiconductor memory element, the SMID, has been proposed for scratch pad storage. The topology of the storage element is simple in nature. Monolithic integrated circuit techniques have been applied in fabricating the element. In a small experimental memory, read cycle times of the 100 ns have been achieved, making the SMID potentially one of the fastest scratch pad memories available for avionics applications.

The basic storage element is shown in Figure 2-51. The functions of the constituent parts of the storage element are as follows: the conductance or non-conductance of the transistor latching pair, $Q_1 - Q_2$, constitutes the fundamental storage mechanism, with the conducting state corresponding to a stored "one" and the non-conducting state corresponding to a "zero". Diode D_1 is used to sense the state of the latching pair. Transistor Q_3 serves to switch the state of the latching transistor pair.

Operation of the SMID memory system is shown in Figure 2-52. Assume that all the memory elements shown in the figure are initially in the zero state and that the following data is to be written into word two - 1000 0. This is accomplished as follows: the information driver for bit one only is switched from -V to ground. Simultaneously with this, the output of the word driver for word two is switched from ground to -V volts causing Q_3 to saturate. Current now flows in the transistor pair $Q_1 - Q_2$ of word two-bit one. Once the transistor pair has latched on, the read/write switch Q_6 is turned off (note that Q_4 continues to have base drive except during clear).

The output is sensed by the sense switches. During read, the word drive for word 2 is again switched from ground to -V volts. Due to the fact that the transistor latching pair of bit 1 of word 2 is conducting, the base of



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Figure 2-51. The Basic Element

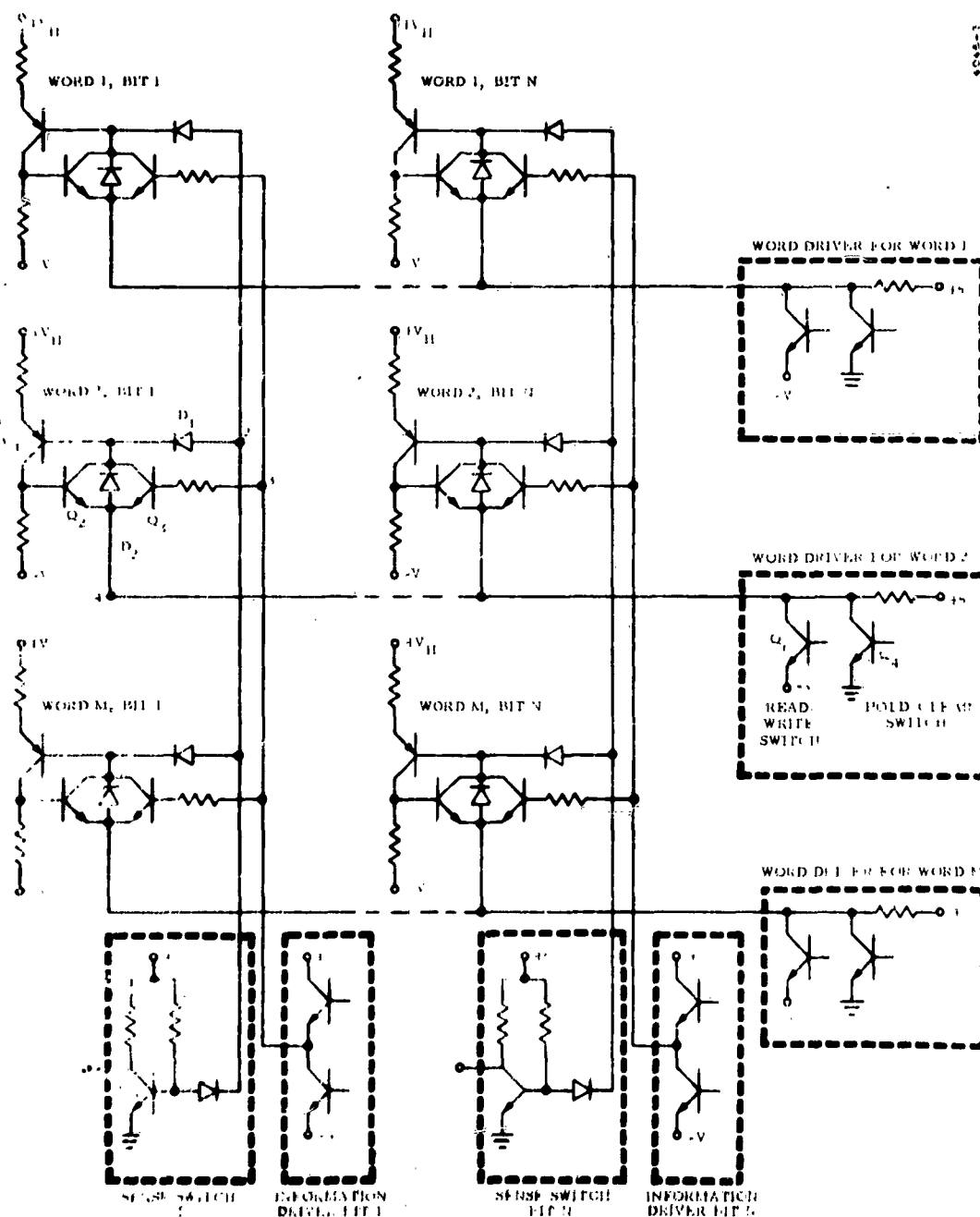


Figure 2-52. Typical SMID Memory System

switch transistor Q_5 is pulled down to a voltage causing it to cut off. The read operation is non-destructive since, at the termination of the read, Q_6 is switched off and holding current once again flows through the latching transistor and into transistor Q_4 . Access time is determined by the external word electronics since the amount of time to switch on diode D_1 and Q_5 when reading a "one" is only of the order of a few nanoseconds.

A memory chip containing nine storage elements may be packaged in a standard fourteen-lead flat package. All of the external electronic functions required to operate the memory are performed by a single type of monolithic integrated circuit. Advanced chip interconnection techniques, now under development, will do much to increase system reliability by reducing interconnections and also decrease system cost and volume. One approach is through the technique of glass sealing of the individual circuit chips, thereby eliminating the need for hermetic packages. It is also envisaged that a good "flip-chip" type of technique will be developed for interconnecting integrated circuits within the next few years. When these techniques are perfected, it will be possible to mount the SMID integrated circuit chips onto premetallized ceramic wafers. Assuming that a memory element occupies 250 mil^2 and that about 25 percent of the ceramic area would be occupied by memory elements, leaving the rest for interconnections, a single ceramic sheet 1-inch square would contain a complete 64 word/21 bits per word memory. This 1-inch square would also include all of the required drive and sense electronics.

MOS Memory Application

Principles of operation of MOS (Metal-Oxide Semiconductor) have been presented elsewhere in this technology review (see subsection 2.1). The application of batch technology such as MOS to computer memory is a distinct possibility. Heretofore the limitation has been principally economic - the price per flip-flop bit has been greater by an order of magnitude as compared to core storage. This is now subject to reappraisal for the same reasons as indicated with respect to logic.

A suitable vehicle for studying the application to memory would be a chip of such size as to contain 64 bits of memory. An approximate size would be in the neighborhood of 100 - 200 mils per side. Additionally, it would be highly desirable to perform word selection on the chip. In this way, input leads to the chip would be reduced by the factor $2^n/n$. The advantages of this approach are both economic and increased effectiveness.

Economies in cost and weight result whenever batch fabricated connections within the chip are substituted for external connections. Within the chip, bonding pad area requirements are reduced in the proportion indicated above - together with their area penalty of four to one. Externally, the need for complex wiring laminates is eliminated. As indicated previously, the reduction in external connection requirements also fortuitously contributes to increased reliability.

Further advantages in using MOS logic for memory are derived from the inherent compatibility of logic levels when a single device is used for both. Complex sense amplifiers are not required, resulting in a major cost reduction. The high logic levels of the memory (of the order of 10 volts) imply superior tolerance to noise as contrasted to films, for example, which produce sense signals of the order of 1-5 millivolts. With respect to power supplies, the need for special supplies, unique only to the memory, is eliminated. Finally, it should be possible to exploit the same packaging medium for both memory and logic.

These advantages are sufficiently compelling to deserve immediate attention of the system designer and the memory designer. It is interesting to note that several papers discussing application of integrated circuits to memory are scheduled for presentation at future technical conferences. (1), (2)

2.2.6 Summary and Conclusions

The memory system requirements for avionics computers have been reviewed. This review has included estimates of capacity and speed as well as environmental and reliability requirements.

Current state of the art memories meeting these requirements have been described. These memories are predominantly of the core type. Several examples of the application of thin film memories have also been cited and described.

Finally, the trends in recent memory research have been described. These trends include continued improvement of discrete element memories from a cost, size, power, and reliability standpoint and intensive research in batch fabrication techniques. While this research is primarily directed toward the commercial mass market, its benefit will also filter down to military avionics

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2.3 COMPUTER ORGANIZATION

2.3.1 General

Digital computers which are contained in contemporary avionics systems are predominantly organized on a centralized basis: the computer may be visualized as a single block into which all the avionics data flows, including that derived from sensors, instruments, the operator, etc.; and from it emanates digital control signals to drive various actuators and displays. To achieve the computing speed required, current avionic computers are internally organized in the conventional parallel, general purpose computer configuration with but few exceptions. A block diagram of the central computer organization is shown in Figure 2-53.

Proponents of the central computer philosophy have maintained that it is the most efficient from a hardware standpoint in that a single arithmetic and control unit is time shared for the entire avionics problem. Alternatives to the central computer heretofore at least have required extra equipment which translated into greater weight, volume, and failure rates. (However, the probability of completing the essential parts of a mission, which may be called mission reliability, would be enhanced.) In the typical crowded cockpit environment, the extra volume was simply not available for more sophisticated computer organizations.

The two principal failings of the central avionic computers of current and previous species have been: (1) the lack of "graceful degradation" properties with resultant complete failure in the event of an isolated component failure; (2) the lack of growth capability - inevitably required in real time avionics systems. The problems resulting from these failings have resulted in a search for more suitable computer organization.

An additional reason for seeking new computer organizations is the need for higher program iteration speeds demanded by recent avionic system applications. Higher computing speed requirements have resulted from a combination of high problem dynamics and high static and dynamic accuracy requirements. A recent example where this is the case is in AAFSS (Advanced Aerial Fire Support System).

New computer organizations of higher complexity than the Von Neumann class have been proposed to overcome these difficulties using distribution and redundancy techniques. These organizations are reasonable for future applications on the following basis:

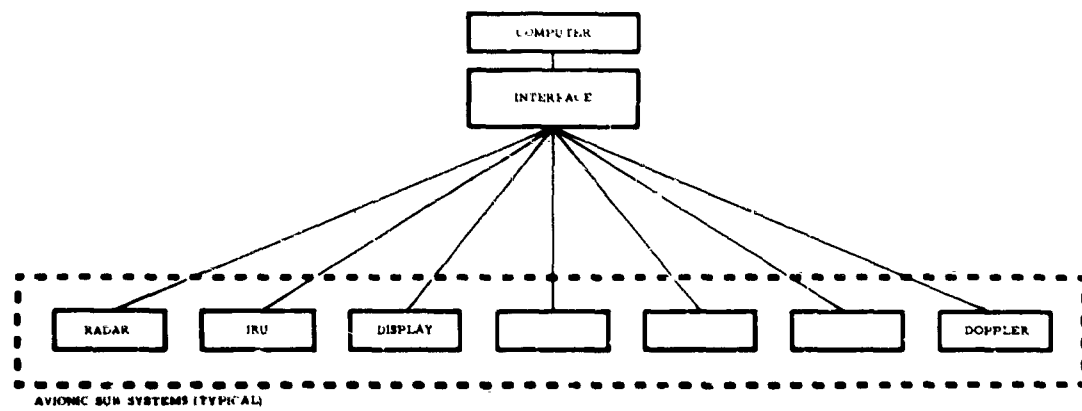
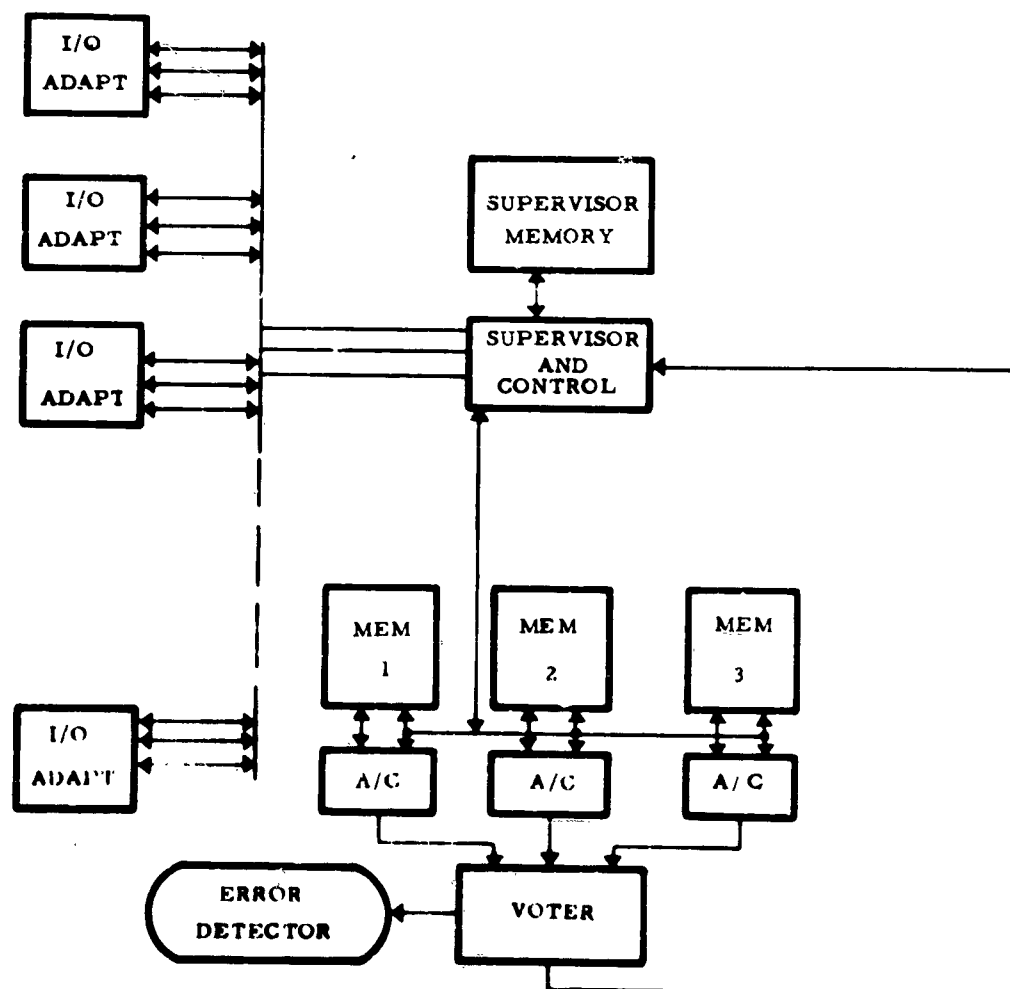


Figure 2-53. Single Central System, Block Diagram

1. Batch fabrication results in reduced cost per logic decision whether measured in terms of dollars, weight, or volume.
2. Batch fabrication has inherently higher reliability. Extensive tests on single chip, multigate packages show an order of magnitude higher reliability than the discrete packaged equivalents. Preliminary data shows the same trend for more complex arrays (i. e. 10^{-7} - 10^{-8} failures per hour). A basic reason for the higher reliability is the reduction in bonding, wiring, and interconnection, which statistically have been prime failure mechanisms.
3. Batch technology offers an advantageous trade-off of increased logic sophistication vs. brute clock speed to achieve increased computing speed. Through techniques as described below, clock speeds, even in the most demanding avionics application, may be maintained in the 500 k Hz - 1 m Hz range. This turns out to be compatible with batch logic designed to achieve highest density on the chip, whether we are considering MOS or bipolar arrays. An added advantage of the lower clock speed is the alleviation of RFI problems - not an inconsequential problem at potential component densities of 10^7 - 10^8 per cubic foot.

Examples of computer organizations exploiting the capabilities of batch technology include the triple redundancy configuration with voting, see Figure 2-54; and the distributed central complex (CCC), Figure 2-55, which illustrates an application to an avionics system. In the distributed CCC, major avionic functions are assigned to independent computers, which except for stored program, are identical in every respect. (Another term which has been applied to describe distributed systems is "functional modularity." Functional modularity provides many system advantages, which will be explained shortly.) In addition to its operational program, each module periodically performs a test problem. The results of the test problem computation are monitored by a central supervisor, made highly reliable through inherent simplicity of design and redundancy techniques.

The computing modules may be standard type GP, GP with DDA, GP with CORDIC, SOLOMON (Simultaneous Operations Linked Ordinal Modular Network), or the Litton Dinary. The SOLOMON and Dinary computers are significantly different from conventionally organized computers. They involve the interconnection and programming, under the supervision of a common control, of many identical processing elements. Each processing element is essentially the equivalent of an arithmetic unit. The result is



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Figure 2-54. Tripple Redundancy Configuration With Voter

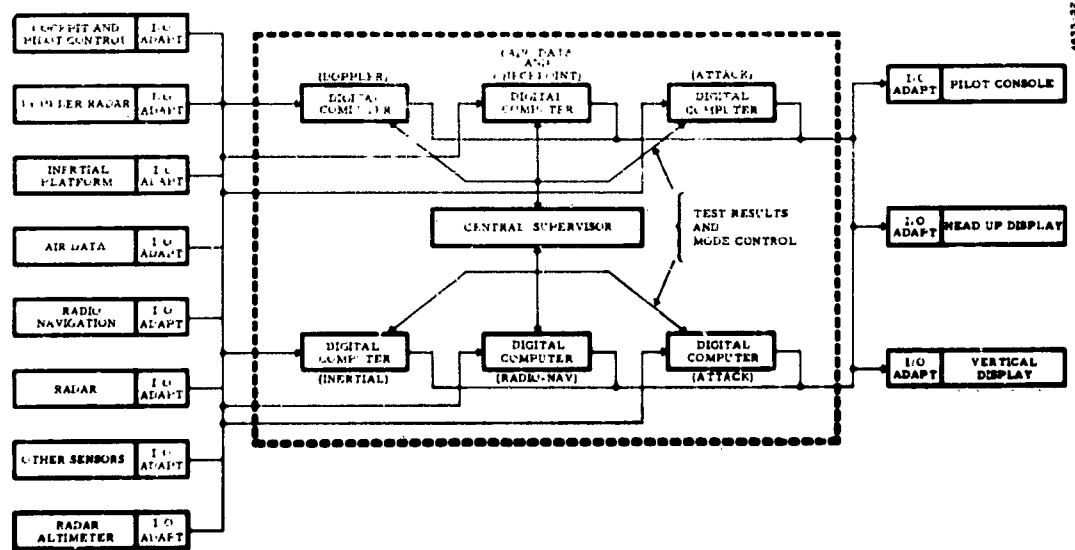


Figure 2-55. Distributed Central Computer Complex

a potential order of magnitude increase in computing speed. Significantly, neither the SOLOMON nor Dinary are new organizations. They have become practical for avionics applications because of the increased logic capability contained on the semiconductor chip.

With respect to failure immunity, the distributed CCC presents several alternatives. However, it is obvious that an isolated failure will at most cause loss of a single function. If this function is not vital to mission success, it may be accepted as a minor system degradation. If the function is vital, one recourse is to provide it within the operating program of another functional module. This subject will be treated in greater detail in the sequel.

2.3.2 Functional Modularity

In a computer based upon functional modularity, separate functions such as navigation, terrain following, etc., are performed by physically separated units. These units ideally are able to perform all their computations utilizing sensor data directly so that in general they do not depend upon results obtained by another module.

This separateness carries with it many advantages especially when applied to large systems. The main advantages are: (1) versatility, (2) fault detection and correction, (3) programming ease, (4) maintenance, (5) logistics, and (6) reliability.

Versatility

Functional modularity permits the system to grow by adding computing modules and enables the system or parts of it to be applied to other aircraft. For some missions, for example, certain unnecessary avionics gear can be removed by simply disconnecting and withdrawing it.

This versatility also allows the individual modules to be used in a much larger range of new applications. In the earlier single central computer approach, a single large scale computing facility having a single arithmetic unit with a highly parallel structure performed all the computations required of the system. It has historically been the case that, in general, for each new system requiring digital computation, the centralized computer complex has either been too large in terms of weight and volume, or too slow in terms of performance. Thus the iteration rate required by the system could not be supplied.

It goes without saying that an ideal digital computer should be of such a nature that it could be used in new applications as they arise without necessity for a costly and time-consuming redesign. Ideally the functional module approach should be easy to program and check out. It can then be applied to new problems and systems without costly hardware redesign and checkout.

In many cases in the past the logical design of a machine has also been such as to preclude any reapplication to new problems. This inability to accommodate new applications without hardware redesign occurs in so-called special purpose computers. Wired-in programs, in particular, have this limitation. Ultimately, when a particular system is altered due to any number of causes, the wired-in programmed computer must be discarded and a new one built. It is an undeniable fact that "hard programming" in which individual units must be disassembled is always harder to do (in terms of money and time). It has also been the case that when the unit is opened, chance accidental failures are the rule rather than the exception.

In conclusion, true versatility is obtained through functional modularity. Since many smaller, identical functional modules make up the central processing unit, it is possible to alter the mix of these modules without difficulty. The ability to reprogram the modules with a minimum of difficulty through the use of "software" rather than "hardware" is an essential part of the versatility inherent in the functional modules.

Another important consideration is producibility. This characteristic is achieved in part through the versatility of the functional modular approach which allows previously developed and perfected hardware to be used in new systems without any physical alteration of the equipment.

Since several identical modules replace a single central computer (provided they can be programmed), a higher production volume results for a given system. Larger volume translates into more efficiency and lower costs. The simplicity of the smaller functional modules and their larger production volume therefore translates into greater producibility.

Fault Detection and Correction

A self-adaptive, or self-healing, feature in a computer complex offsets critical failures in computation or sensing. With this so-called configuration control, identical computing elements normally devoted to lesser

functions automatically can be pre-empted to maintain critical functions, when elements normally performing these fail. If a malfunction occurs at an alternate sensor. This action is achieved by controlling the settings of gates located at strategic points in the computing networks. Failure in the primary navigation mode, for example, might result in a shift into a dead-reckoning navigation mode.

Configuration control endows the computer complex with what appears to be the good fortune of having its failures always occur where they matter least. In the event of failure of a particular functional module, the self-adaptive or self-healing feature can be brought into play through altering the program of other parts of the central processing unit. For example, if the functional module performing a critical computation should fail, the sensors supplying the basic data may still be working. In this event the self-healing feature requires that one of the other functional modules drop some of its less essential operations and take over the critical computation.

Thus the self-healing feature cannot be properly exercised unless the system is capable of altering its own program. Such an alteration of the program cannot be achieved in hard wired systems in which the program connections are permanently determined through direct wiring between units unless extra equipment is held in standby status at all times.

Computer self test is used to determine the failed functional module or sensor. The nature of the failure is indicated to the pilot and is also available to the maintenance and service personnel. This greatly simplifies the maintenance and servicing of the equipment. In the earlier single central computer, the failure of this computer effectively stopped all computer activity so that fault indication was not possible. The functional modular approach allows the partially working system to pinpoint the location and nature of the failure. Correction is achieved through easy insertion of a new working module.

While this concept has been primarily intended for implementation in a ground environment, a second possibility is that the malfunctioning module is replaced by a spare module while the mission is in progress. This is particularly attractive in systems with long mission times. The required operating program can then be inserted via tape or other bulk storage in the case of nonpermanent memory.

Programming Ease

Another aspect of the functional modular approach is the ease of program checkout. In the case of the single central computer, simulation on a commercially available computer can be used to eliminate gross programming errors. In the final analysis, however, it is necessary that all parts of the program work together on a single central processor.

With a single arithmetic unit a queuing problem is generated in which machine time in program checkout is difficult to obtain. Also, all the programming must of necessity be done by personnel physically located at the same facility. A breakdown in the single central processor automatically stops all program checkout efforts. This invariably lengthens the time necessary to complete the program checkout. Note that this limitation applies to redundant computer systems also.

In the distributed or functional modular approach, many individual computers (functional modules) replace the single immense central computer. During program checkouts these separate computers can be used in physically separate locations. Because of their lower cost, more can be made available for program checkout. Failure of any individual computer does not automatically stop the entire program checkout effort.

Furthermore, the programs written for the individual systems are simpler in nature. Interaction between the individual computers is minimized, and a much more efficient program generation and verification process is achieved.

Program checkout is necessary in both "soft" and "hard" wired programs. Direct wiring between computing elements does not eliminate the necessity of the verification of the correctness of the connections. Errors in the hard wired programs are much more difficult to correct since they involve actual physical change in the system rather than a mere alteration of the contents of a memory cell.

Maintenance

In advanced avionic system, automatic fault location should be carried to the unit level and fault isolation carried to the module level without the need of test equipment on the flight line.

Maintainability and serviceability are greatly enhanced by a functionally modular system. A central computer complex made up of a number of autonomous computers is capable of effective operation even though one of its members is out of action. The remaining elements can easily be made to recognize and pinpoint the failure of any one of the functional modules.

Hard wiring in which direct wired connections make each functional module unique complicates maintenance. This happens in the repair of the individual modules when the unique wiring of each unit prevents the use of a universal approach to fault isolation within a unit after removal from the flight line. Maintenance procedures are complicated since a different problem is presented by each unit.

If the modules are programmable using software, a universal functional module is used for all the elements in the system. Repair is standardized and is simple when compared to the larger single central computer. Replacement is made easy by the fact that the individual computer modules are identical and relatively small compared to the large single central computer.

Logistics

The functional modular approach greatly simplifies the supply and inventory problems. If the functional module is programmable, it can be used in a variety of applications without requiring any hardware changes. The total inventory is reduced since the single universal functional module is used in a multitude of applications. Each functional module is small when compared to the large central computer.

Much of this advantage is lost when direct wiring between computing elements is used since each functional module is now unique and must be stocked separately.

Reliability in Functional Modular vs Redundant Systems

Reliability can refer to the probability that the mission will be accomplished disregarding the number of component failures, or it can refer specifically to the component failures. The former has been called mission reliability while the latter, system reliability.

The functional modular approach emphasizes the mission reliability. Thus even though parts of the system fail, the mission (which might be to bomb, intercept, etc.) is not a failure, since vital computations can be continued in other parts of the system in the event of the failure of a particular functional module.

The ability to put aside parts of the problem in the event of a failure to assure vital computations is an inherent characteristic in computers which can change their own program. The ability to change the program so that different computations are performed is not present in systems where the connections between computing blocks are made permanent through the use of direct wiring.

Redundancy has also been used to obtain higher mission reliability at the expense of system reliability. Redundant systems require more equipment than non-redundant systems. Since the failure rate of an aggregate of individual elements is directly proportional to the total number of such elements, the redundant approach, while giving a higher mission reliability, has the drawback of having a lower system reliability. The large number of failures which occur in large systems translates into greater maintenance problems and eventually into life cost of the system. In addition to this, redundancy adds weight and volume.

The functional modular avionics computer complex has the virtue of greatly increasing the probability that the essential parts of the mission will be accomplished (mission reliability) without causing a corresponding decrease in the system reliability compared to redundancy in which all parts of the problem are repeated.

2.3.3 Application of Large-Scale Integrated-Circuit Arrays

The successful development, and production of silicon integrated circuitry has proven this technology capable of providing an order of magnitude improvement in reliability of systems. Concurrent with this improvement in reliability has been a continuing reduction in circuit function cost. The increased reliability of IC's indicates that predominant failures are associated with bonding and lead failures within the circuit and multilayer wiring board or interconnection failures at the system level. These failures can be further eliminated both by reduction of the circuit to circuit transfers required external to the silicon wafer and a reduction in the

number of connections required at the subsystem level. This in turn will greatly reduce the number of individual packages with their associated input-output terminations. Thus it is readily apparent that if these higher order circuit functions can be achieved, today's level of reliability, cost and size reduction can be further improved.

For the 1973-1978 time frame, avionic computers should have as much as a ten to one improvement in reliability over that presently available with today's integrated circuit capability. Additionally, enhanced subsystem performance and an overall cost reduction will be realized. These improvements will be accomplished through the sophisticated use of a large scale monolithic integrated circuit arrays containing up to 1,000 circuits utilizing either metal-oxide-semiconductor (MOS) or bipolar active devices.

The microelectronic market is extremely competitive and is indicating a downward trend as various suppliers attempt to strengthen their position and enlarge their share of the market. This, in itself, is sufficient to enable decreasing per-piece cost projections under conditions of increasing demand. Other factors that contribute to reductions in the total cost of a microelectronic system lie in cost savings which can be achieved in engineering, reliability, and assembly time.

New processes and technologies will cause sharp reductions in price per circuit functions in the near future. The tendency toward more functions per package, greater masking definition, and new technologies, like MOS with its extremely high yield factor, are all under current development and portend a reduction of hardware costs at least a full order of magnitude.

2.3.4 Logic Design Problems Using Large IC Arrays

The increased logic capability of the building block presents new problems in terms of system partitioning and logic selection for the avionics computer. A brief review of these problems follows:

System Partitioning

The goal of system partitioning is minimizing the number and types of building blocks. This is a major problem area and will require the most careful appraisal because of its direct effect on cost, logistics, and

maintenance. In previous computer systems, this problem was minimal because a few basic gate packages could be deployed throughout the computer with usage frequencies of the order of 50-60 percent. The gates were then interconnected by a laminate, wiring panel, etc. to achieve the desired logic configuration.

In the batch fabricated building block, a chip 100 x 100 mils square contains several hundred active devices. Obviously, the majority of these must be interconnected on the chip which thus becomes a unique logical structure. No package could accommodate the leads otherwise required. As an example, a gate with fan-in 4 requires 7 terminals. Ten such gates would require a minimum of 52 terminals — which no known package provides. Even if it were available, such a package would be contraindicated both by reliability considerations and efficient use of the chip (bonding pads represent waste area).

Thus, the building-block level must contain a logic subfunction. Examples are registers, adders, counters, integrators, etc., or major whole bit functions thereof. This approach is relevant not only to the era of several hundred components per chip, but also to near future (1-2 years) monolithic devices with 20-30 active components which may be organized into half or whole bit configurations.

Logic Selection

The superiority of TTL logic forms for monolithic bipolar and MOS technology has been well established on a cost-performance basis (see section on Logic). Where higher speed is required, all indications are that bipolar transistors with beam lead or dielectric isolation techniques will provide nanosecond switching speeds. Higher speeds should also be realizable with MOS using CML (current mode logic) configurations — though no such devices are currently on the market.

Serial logic has several advantages for batch fabricated arrays. First, it drastically reduces the package terminal requirements. Secondly, one bit of clocked delay occupies less area on the chip by a factor of six to one as compared to a static register stage. These are important advantages for DDA, Dinary, and other organizations of this generic class which are essentially serial in nature.

So-called word-parallel, bit serial intercommunications are also favored for these same reasons. Moreover, simple transmission tests may be utilized as well as redundancy to maintain complete self-test of this important area.

Logistics and Maintenance Constraints on Logic Design

Several aspects of logistics were discussed in the preceeding: (1) minimizing the number of building blocks; (2) minimizing types of building blocks. These may be shown to be a function of machine type and system partitioning. In machines of the Von Neumann (G. P.) class, typical spares requirements currently run 10-15 percent. This figure will frequently rise to 50 percent and higher in the batch computer because of the greatly reduced number of primary building blocks.

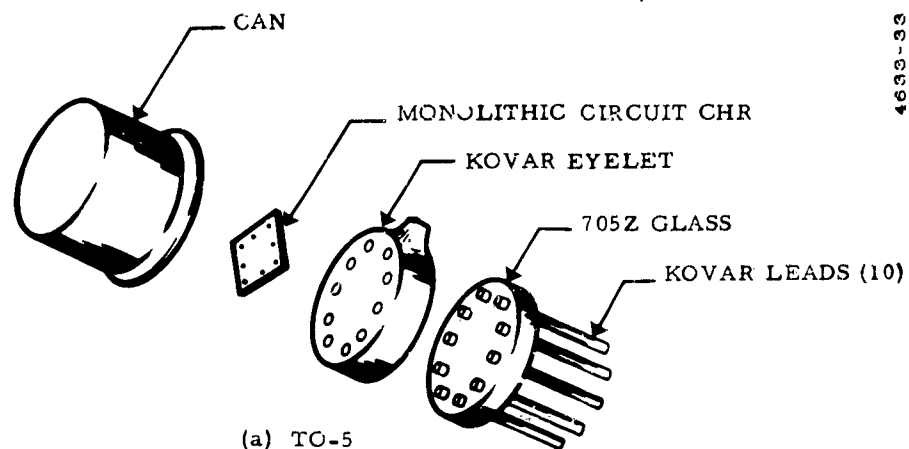
Another consideration is the throw-away cost of the complex array on a 100 x 100 mil chip. The production cost is a direct function of chip size and only a weak function of complexity. Once the tooling cost has been amortized, cost of the complex ship should not be grossly in excess of current multigate packages, i. e., \$5 to \$10. However, the tooling for typical module will run between \$20,000 to \$30,000. In avionics, where at least initially production runs are small, this places a premium on system designs which minimize the number of building block types.

The functional packaging previously recommended as an aid to minimizing the number of package types is also advantageous from maintenance considerations. Far fewer test steps are required to test a complete logic function (or several complete bits thereof) than the individual discrete components. Moreover, the lower cost per logic decision through batch technology implies that 100 percent self-test should be the goal in those areas not conveniently tested by software. Techniques accomplishing this include majority voting, parity, and more sophisticated error detection codes.

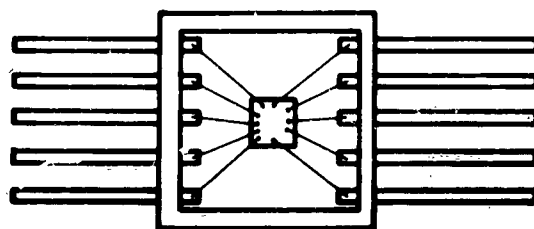
2.3.5 Packaging

Figure 2-56 shows current examples of digital packaging. Included are the standard TO-5 can variations; the more recent flat packs; and the flip-chip, or upside down mounting. The trend to elimination of the conventional hermetically sealed header is evident. In the flip-chip, this is accomplished through glass passivation of the chip. Such packages

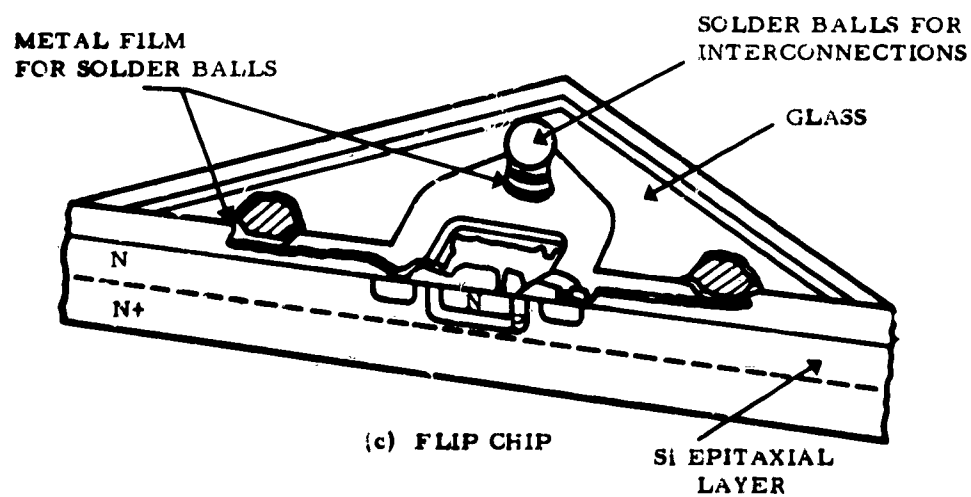
4633-33



(a) TO-5



(b) FLAT PACK



(c) FLIP CHIP

Figure 2-56. Packaging Examples

result in significantly lower cost. The most severe test for the glass package is that of chemical stability with respect to water. This has been proven in over 200 million component hours of tests, including exposure to boiling water, to steam at 400°C, and to an ambient of 85°C and 85 percent relative humidity.

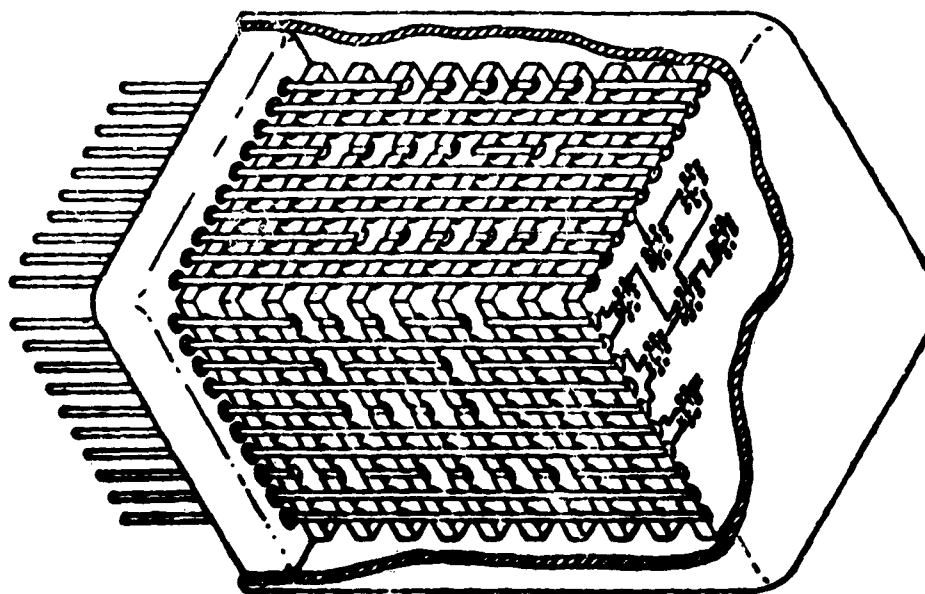
Future packaging densities as high as 10^8 components per cubic foot will be used in the 1973-1978 avionics computer. To achieve such densities will require a departure from current planar packaging and the exploitation of three-dimensional packaging. One technique for accomplishing this is a straightforward extension of the micromodule concept. Instead of discrete components being mounted on the ceramic wafers of the micromodules, we could mount the 100 x 100 mil chips of logical sub-functions - each protected by glass encapsulation. Figure 2-57 shows a possible configuration.

2.3.6 Logical Organization of Circa 1970 Avionics Computers

Figure 2-58 shows the organization of an avionics computer complex representative of the next generation of avionics systems. Currently two development programs are in progress which have as a principal goal the achievement of such functionally modular computer systems: the ILAAS and the IHAS.

The computer complex consists of a Central Processing Unit (CPU) and a Signal Transfer Unit (STU). Together the CPU and STU perform and control all computations between the transfer devices, sensors, and the displays and controls. The Central Processing Unit is capable of performing all the arithmetic operations and performs all computations by means of functional modules. The STU performs, at the operator's option, the mode selection and establishes the alternate modes of operation of the entire avionics system as a function of automatic fault isolation and airborne performance monitoring. The structure of the 1973-1978 avionics computer will most likely retain this basic organization. However, a unique logical design to be discussed in a subsequent section will result in a many fold increase in the performance effectiveness of the computer complex.

Other features of this computer organization are as follows. The computer central complex is modularized on a subsystem computational functional basis. Modules not required for a specific mission may be



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Figure 2-57. Three-Dimensional Packaging

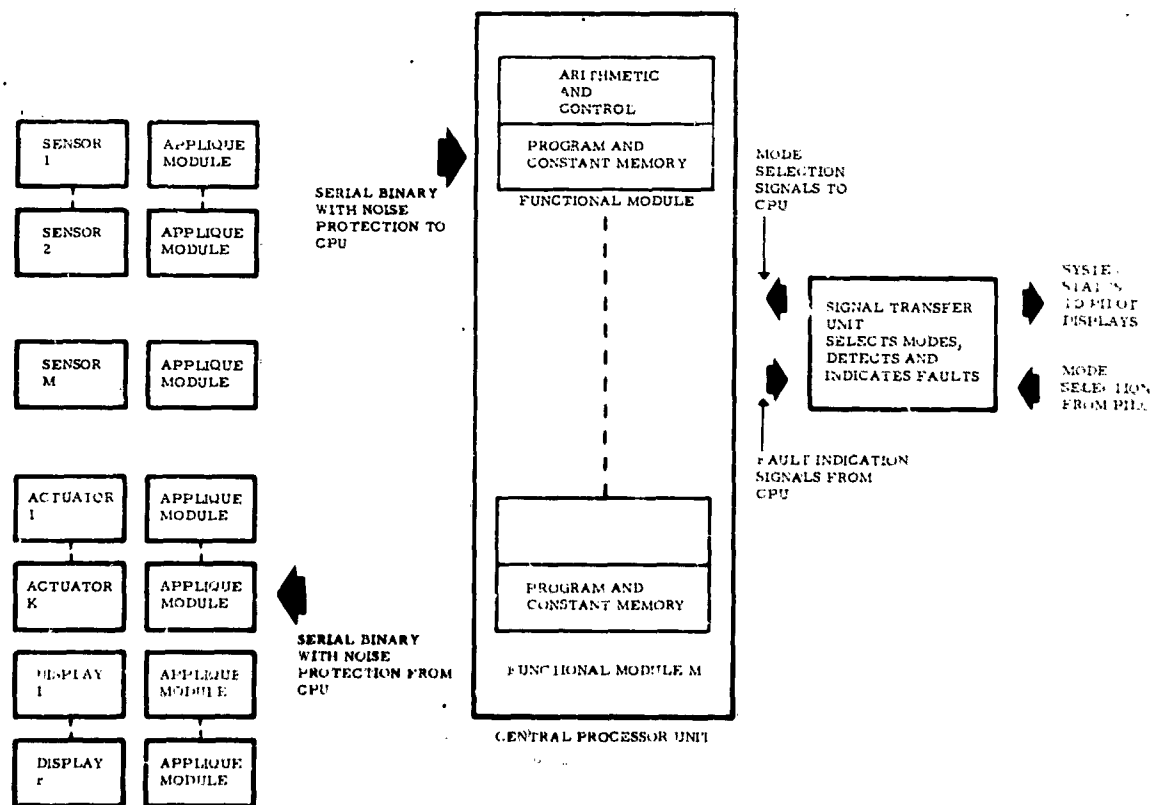


Figure 2-58. Block Diagram of the Computer Complex

removed without affecting the operation of, or requiring changes in, the remaining system. The computer central complex interface is via applique units located remotely at the sensors. Transmission of the inputs and outputs is in a bit serial and word parallel format. The CPU checks validity of information received using odd parity, complementing, or appropriate error checks such as reasonableness.

2.3.7 Block-Oriented Logical Organizations

With a realization of the potential improvements in reliability, performance, and cost inherent to larger arrays of integrated circuits, the question which arises is: which logic organization shall be standardized for the 1973-1978 avionics computer. As indicated in the preceding, an important criterion for evaluating different logic organizations is the facility with which they utilize the large complex chips which will be available in that time period. There are two important indices in this regard:

1. The logical organization should be made up of an array of identical structures
2. These structures must have a minimum number of leads leaving and entering.

Any computer organization which uses elements possessing both these properties can be called "block-oriented".

Figure 2-59 shows a general block diagram for the 1973-1978 avionics computer. The principal difference between this diagram and the Figure 2-58 it may be noted, is the replacement of the centralized arithmetic and control with a 10×10 array of computing blocks within each module. Each of these computing blocks is identical. Each block consists of a single complex chip which is the equivalent of an entire arithmetic unit. Thus a single functional module will represent, in effect, a parallel arrangement of 100 computers. The result is a powerful enhancement of the computing speed, input-output capability, system monitoring capability, etc. Yet, because each chip is no larger than today's flat pack, the weight and volume will be that of a conventional machine. We shall examine the various logical organizations currently available relative to their suitability for this advanced computer concept.

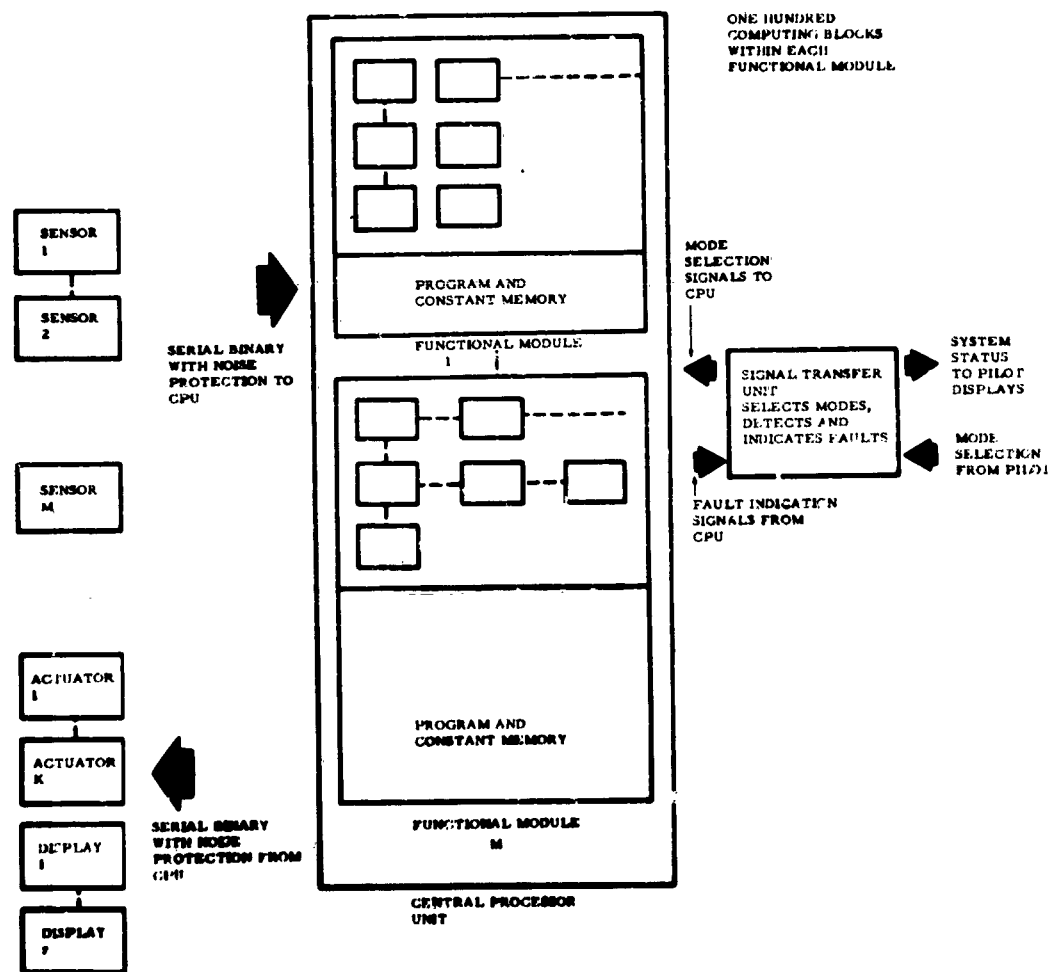


Figure 2-59. Block Diagram of 1973-1978 Computer Complex

The Digital Integrator as a Block-Oriented Element

The digital integrator can be used to fabricate entire digital computers, and this has been done in the past. One missile computer, to cite an example, was made in this manner. The individual digital integrators were fabricated using core shift registers and conventional lumped circuit elements. This particular machine was built over five years ago.

A digital differential analyzer is an example of a "block-oriented logical structure". The digital integrator, if properly designed, would have not many more leads coming into and out of it than a flip-flop. An entire digital computer could be fabricated using only this element.

The digital integrator, however, has many shortcomings when applied to problems normally assigned to the standard general purpose computer. Typical of these shortcomings are the following:

1. In handling highly uncorrelated data, one problem is the size of the increment which must be used to track. This limits the accuracy to which a given variable can be handled within the DDA.
2. The initial acquisition of a target requires high tracking rates unless the computer is allowed to limit the system operation.
3. In the event such a fixed increment integrator "drops a bit" a complete disorganization may arise in the machine which may not be immediately discovered and which is difficult if not impossible to correct. In real-time applications, this is catastrophic.
4. The fixed increment integrator is weak in mode changing and branching. All parts of a given problem must be active at all times to track the problem even though all may not be required at any time. This burdens the arithmetic capability of the machine.
5. The DDA is completely lacking such vital functions as indirect addressing and table look-up.

The requirement that all the computations in the problem be active at the same time implies at least one integrator for each function. For small problems where high iteration rates are desired, a 10×10 array of digital integrators should be adequate. Larger problems, such as bombing, fire control, etc, in which hundreds of multiplications, divisions, etc, are required, would entail more capacity. Adding more integrators would increase the failure rate of the system and the reliability would suffer.

Conventional general-purpose computers typically time-share the arithmetic capability for a multitude of computations. However, time sharing of this sort in the DDA would mean that a given integrator would be shared among several computations. The inherent weakness of the integrator in mode changing severely limits its application in operations of this type. Several seconds might elapse in the worst case before the computer would be able to reestablish its outputs when changing modes.

Because of these weaknesses, the digital integrator has never gained wide acceptance as a general-purpose digital computer. Generally when it is used, a standard whole-number digital computer is used in conjunction with it to provide the initialization and decision-making functions.

For the reasons given above, the digital integrator as utilized in the DDA would seem not to be acceptable as the general-purpose computing element for an advanced avionic system. Its range of applicability is too narrow.

The Standard Whole-Number General-Purpose Computer

The typical general-purpose whole-number computer possesses a single arithmetic unit which is time-shared among many computations. In order to obtain the iteration rates required in most problems, highly parallel logical designs are used, and a great number of individual, high-speed circuit elements are required.

If we attempt to mechanize such a highly parallel computer from large scale integrated circuit arrays utilizing present computer organization concepts, we immediately encounter two obstacles. First, a large number of leads will be required to interconnect each silicon chip with the other chips in the computer. There would be no room to make these connections around the periphery of the chip. The package enclosing the chip would be unreliable due to the large number of leads and lead seals. Second, each complex function would be unique within the computer. The computer design would require the development of a great many (the order of 50) integrated circuit types. The great expense of this initial development and the following production of many different types of circuits will greatly reduce, if not entirely eliminate, the potential economic advantage.

In brief, the typical general-purpose digital computer is not block-oriented.

The Solomon Computer

In the Solomon computing concept, a multitude of simple arithmetic elements are used to perform the totality of computations required for the problem. In problems of the sort originally proposed for the Solomon computer, namely field problems, a real increase in computation ability is achieved by this organization due to its parallel mode of operation.

Such a machine is block-oriented, since each arithmetic unit could be fabricated as a single element in a 10×10 array. All elements would be the same, and the number of leads into such an element would be small.

Figure 2-60 is a generalized block diagram of the Solomon system. The program memory contains the program commands. These are retrieved, indexed, and distributed via the control unit to either the network sequencer or the input-output unit. The I-O unit is comprised of a primary and secondary exchange. The primary exchange operates at data rates substantially the same as the processing element network, while the secondary exchange operates at speeds compatible with most peripheral devices.

In a more conventional computing problem, such as navigation, guidance, or terrain-following, the Solomon principle runs into great problems. These problems arise due to the basic inability of such a machine to handle intermediate products in a computation. For example, if the output of arithmetic unit number 26 is to be used in arithmetic units 36, 40, 51, and 74, how is the communication of this result to these elements to take place? One might picture a rather elaborate scratch pad to perform this.

Another possibility would be direct or "hard" wiring. If hard wiring is used, the comments made with respect to the digital integrator would then apply: if the problem is too large, the 100 arithmetic units might have to be time-shared among more than one computation. This would mean mode changing, and once a wire is hard-wired from point A to point B, no mere program branch is going to change it. Thus a hard-wired Solomon array would be severely limited in the size of problems it could handle for this reason.

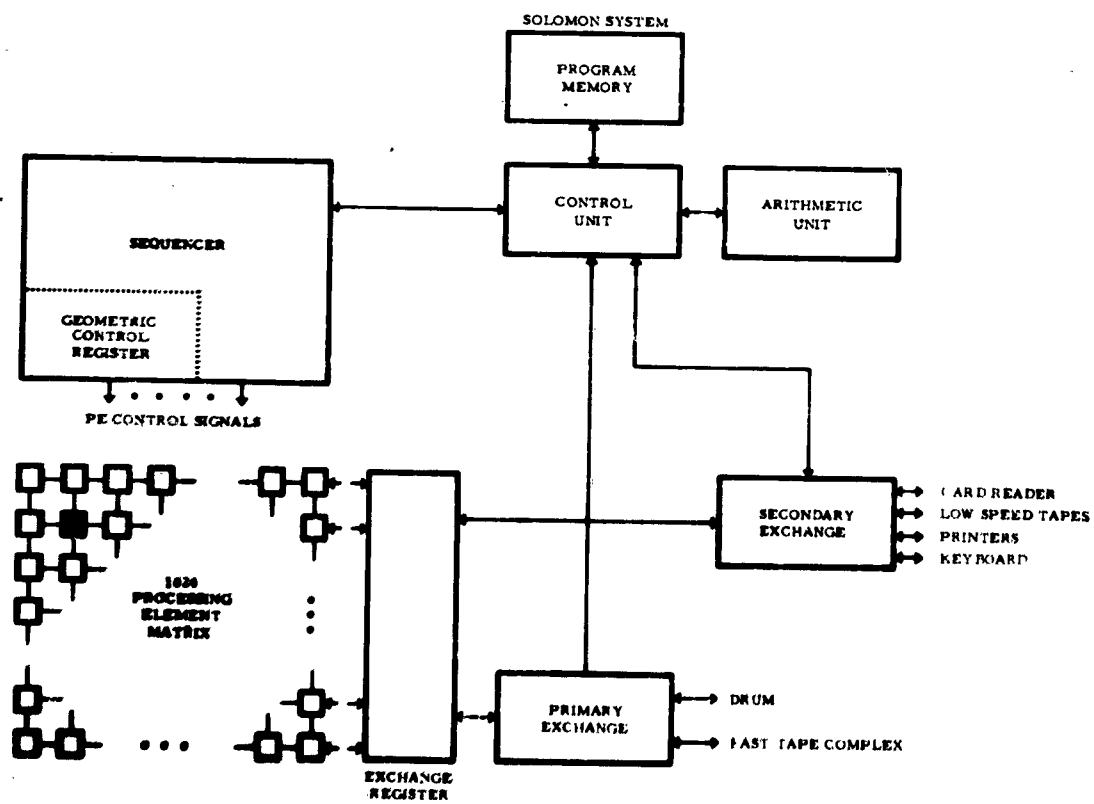


Figure 2-60. Solomon System

Another difficulty in the Solomon principle is that in a chain of computations where the result of each must be developed before the next can be started, such as the product ABCDEF, a large delay will develop due to the necessity for doing the multiplications in sequence. Thus the highly parallel organization of the Solomon computer system would still have the delays which result from the conventional single arithmetic unit structure.

The Solomon system cannot take full advantage of the full operative speed of 100 arithmetic units operating in parallel. However, the Solomon computing system comes close to satisfying the requirements of the large scale integrated circuit array. Its organization is block-oriented, and it does not have the inherent weaknesses of the conventional digital integrator. Time sharing of a 10×10 array of arithmetic units would be possible since at the end of each major program cycle, when all the products and quotients were completed, the elements would then be available for a new program arrangement which could work on the results of the computation.

The main weakness of the Solomon concept lies in its inability to come to grips with what might be called the "scratch pad" problem. The problem is how to handle intermediate products in the computation. It is possible to conceive of a very elaborate scratch pad memory into which the outputs of all 100 elements would be placed. Then at the beginning of the next major program cycle each of the 100 elements would address the scratch pad for the number it required. This scratch pad would then consist of 100 words of random access memory. In order that the 100 elements in the array all be able to address the scratch pad at the same time each would have to possess a complete addressing system able to work independently from all the other addressing systems. Such a scratch pad memory, needless to say, would require excessive equipment.

Dinary Computer

The "dinary" computer combines the restoring type iteration capabilities of the "whole number" binary computer with a simple intramachine communication mechanism of the DDA type computer.

Applying the dinary concept to a machine built of MOS chips, for example, would provide an extremely fast computer. This result obtains because the dinary blocks can be connected together to operate in parallel, rather than in serial fashion.

With a parallel dinary machine, a considerable reduction in storage space obtains because intermediate solutions within an entire programmed set of equations do not exist as such and do not have to be stored in a scratch pad for later call-up.

This computer philosophy is block-oriented, just as the Solomon is, but it has none of the weaknesses enumerated for that computing principle. In the Solomon system intermediate results are not used until the end of each major cycle when all the multiplications, etc, are completed. In the dinary system, intermediate results are communicated in the form of three valued increments of varying weight (hence the name "power increment") at each minor iteration of the process. These increments are much easier to handle than would be the whole numbers produced by the Solomon system.

The scratch pad problem is completely lacking in the dinary computer. In a 10×10 array of power increment computing blocks, complete intercommunication between any two blocks takes place continuously rather than at the end of the major iteration. Thus the intermediate results are immediately used in the computation process rather than having to be stored in some sort of scratch pad memory. Thus no hardware external to the 10×10 array is required for the storage of intermediate results because such results never exist as whole numbers.

Since it is possible for any block to communicate its contents to any other block in the array using the "power increments", it might be said that in the dinary computing system the arithmetic units themselves provide the scratch pad memory between major iterations of the computer. Yet since the arithmetic register are contained in the individual cells, no external scratch pad is present.

Unlike the DDA, the dinary computer lends itself readily to mode changing. This is true for the same reason that the Solomon system can change modes: at the end of each major iteration the elements have whole number results and have completed the computation. The dinary

computer can have such vital functions as indirect addressing (which in effect gives the index register capability), and table look-up (necessary for ballistic computations of any nature).

Unlike the DDA which carries any intermediate errors permanently in the computation, the dinary computer starts with fresh data at the beginning of each major iteration, just as the Solomon system. Thus such errors are almost immediately eliminated from the system.

However, in some cases (mainly input-output) integrators do have certain desirable features. Due to the almost identical structure of the DDA and dinary block, it is possible to arrange the logic design so that a particular block could operate in either mode (DDA or dinary) depending upon the program of the computer.

In conclusion, the dinary computing system is block oriented and possesses none of the disadvantages normally associated with the other two block oriented computer philosophies, the digital differential analyzer and the Solomon computing system.

2.3.8 Dinary Computer*

In this section the system organization of an advanced avionic computer complex exploiting large integrated circuit arrays and the dinary structure will be discussed.

This computer complex possesses all the advantages of functional modularity enumerated in Section II. These include versatility; fault detection and correction; programming ease; maintenance; logistics; and reliability.

Of fundamental importance, however, is the fact that these advantages have been achieved without the usual hardware penalty associated with functional modularity. This has been accomplished through logical time

*This computer is under development at Litton Industries, Inc., Guidance and Control Systems Division, and is proprietary to Litton. This work was not performed under the contract.

sharing. Since time sharing minimizes equipment requirements, it also lowers failure rates and enhances both the system and mission reliability. Lower failure rates automatically translate into fewer maintenance problems and a lower life cost.

Although functional modularity, in a sense, represents a move away from time sharing, it is still possible within each separate functional module to use this equipment minimizing technique. If a given gate now performs two functions which previously required two gates, a superior system results, provided all the essential advantages of functional modularity are maintained.

Furthermore, through the use of time sharing, the additional hardware required in the failure modes can be minimized. If each functional module can be programmed, parts of the problem can be put aside during the failure modes. In a system which cannot time share, extra equipment must be provided for the failure modes. If the navigation computer fails, for example, the bombing computer might have to have extra equipment to turn on so that this essential operation, or at least parts of it, can be continued. In a failure mode, the dinary computer would not require extra equipment but would simply put unnecessary parts of the problem aside through operation of the program.

Central Processing Unit

The central processing unit of the dinary computer performs all computations by means of functional modules. Each of the functional modules has a block-oriented arithmetic and control array coupled with a program memory. The arithmetic array consists of four rows of 25 elements. Each element is a dinary arithmetic unit with the ability to add, subtract, multiply, divide, etc. The computing blocks can also be operated as DDA integrators or in the CORDIC format for special situations (for example, the use of rate functions for input-output purposes, binary-to-decimal conversion, etc.).

The second part of the system is the memory control logic. This is used to control such operations as conditional and unconditional branching as well as indirect addressing. This is done using information from the arithmetic array and also the read-only memory. It should be emphasized that although the memory control logic is considered separate for conceptual reasons, this part of the system can be distributed among the individual elements in the array and need not exist as separate hardware.

For program storage, a read-only memory is provided. This optimizes speed for a given memory hardware availability.

Communication With The External Equipment

The inputs to the central processor unit are via serial binary numbers. All quantities not satisfying this requirement would be converted at the sensors using suitable means. When the input quantities are received at the central processor unit they are tested for odd parity, complement, and also for reasonableness. One reasonableness test that could be used is a correlation test for the change in a particular variable between samples.

Similarly, outputs from the central processor unit would also be in the standard form mentioned above. These quantities would be serial binary, with noise protection means. At the actuators and displays, these quantities could be converted to the required physical form by suitable devices.

A block-oriented computer system possesses extremely attractive features when considered in relation to the interface problem. Since each of the 100 arithmetic units making up the computer is an independent entity capable of both arithmetic and logical operations, it is possible to handle as many as 100 inputs and 100 outputs by sending only one input and one output into each arithmetic element in the system. A block diagram of the input-output system for a block-oriented computer is shown in Figure 2-61.

There is normally a queuing problem associated with radar data in which a buffer must be constructed in the conventional digital computer due to the essentially serial nature of the single arithmetic unit which must be time shared among all the inputs. In the array-configured processing system with its 100 arithmetic units, each unit only has one input

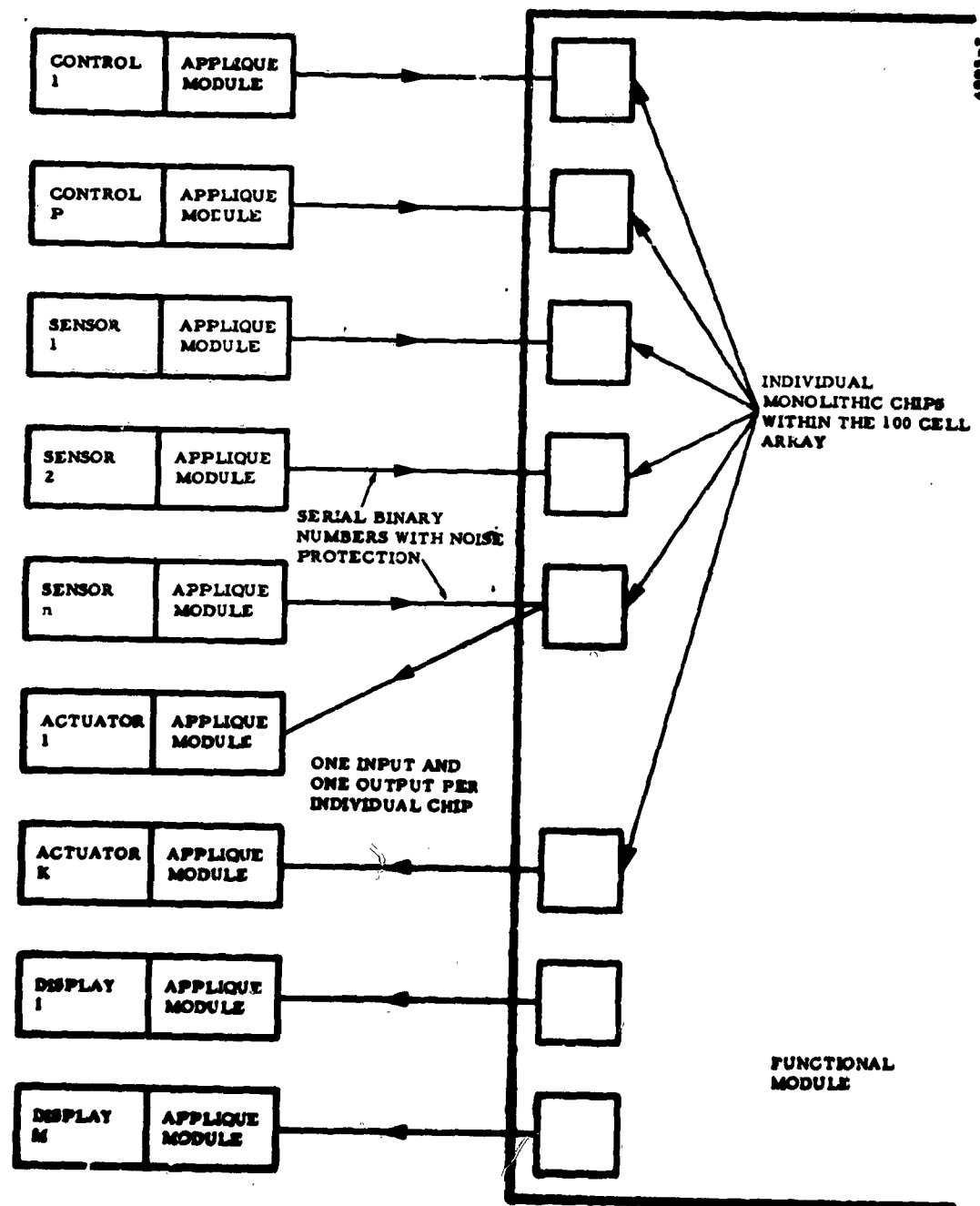


Figure 2-61. Input-Output System

and can accept that input with essentially no delay. Thus, the requirement for the interface buffer is also eliminated by such a computing system since the buffer is, in effect, built directly into the array of arithmetic units which comprise the central processing unit.

In summary, each of the elements in the arithmetic array has one input and one output line. This means the system is capable of handling a total of 100 inputs and 100 outputs. This capacity is quite adequate for almost all problems an avionic computing system might be called upon to handle.

Signal-Transfer Unit

With the binary element, the signal-transfer unit, as indicated previously need only provide the necessary switching and logic circuits for the functions of mode selection and fault location and indication. It also allows the pilot to control selection for the operational and alternate modes of operation of the avionics system. Since its operations in the binary computer are relatively simple, its construction can also be simple, hence reliable. This reliability must be a characteristic of the STU, since it is the one element in the computer complex not constructed on a functionally modular basis.

A block diagram of the signal-transfer unit is shown in Figure 2-62. Triple redundancy on a low level is used to give high reliability. Because of its simplicity, the equipment requirements are low even with the redundancy.

The action of the STU in a fault situation will now be explained. Faults occur in two classes: in the sensors and in the functional modules themselves. Sensor failures are monitored by the functional modules using the programming ability possessed by those units. The STU need only receive information from the functional modules concerning sensor malfunction and transmit it to the pilot.

(The techniques through which digital computers detect sensor malfunction are well known. The odd parity check and the complement checks mentioned earlier detect transmission errors. Reasonableness criteria check both the sensor and the communication means. Comparisons between related sensors, such as doppler and inertial inputs also provides a check).

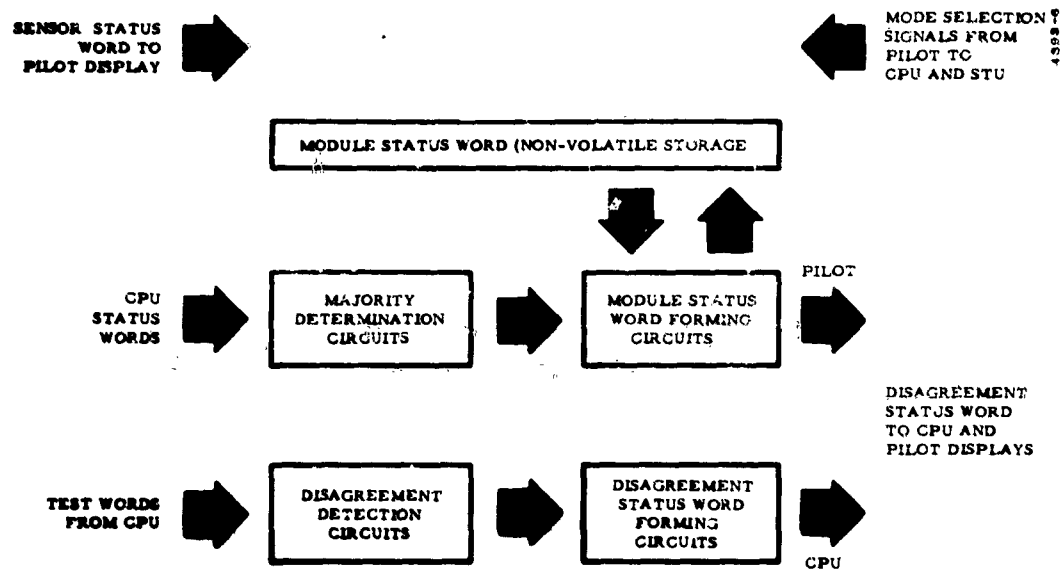


Figure 2-62. Signal Transfer Unit

One cell in each functional module receiving a given input is connected to the STU. Through programming, a status word is constructed in the functional module in which each sensor occupies one bit position. If the sensor is judged operative, that bit position is set to zero. This status word can be transmitted directly through the STU to the pilot's display where each bit can be converted into a sensor status indicator.

Mode-selection signals from the pilot to the individual modules are also sent in the form of status words which are placed into array cells as inputs. Through the usual programming techniques, the individual functional modules are able to interpret the intention of the pilot regarding the use or non-use of the sensors, and adjust their programs accordingly to use or not use a particular sensor.

From the above discussion it is evident that the STU has essentially no involvement with the fault detection and correction in the sensors, except to display the status words generated within the central processing unit.

The failures which occur in the functional modules themselves present a different class of problems. Since any one of the function modules is equally likely to fail as any other, no one can be regarded as superior to any other in the ability to detect faults within the central processing unit (CPU). This, of course, is the justification for the STU.

The STU holds the status of the functional modules in the form of its own status word. As with the sensor status words, each bit position in the status word refers to the operative condition of a particular functional module. This status word is also sent to the pilot display. Based upon the status words, the pilot can remove any functional module from the system. He does this by setting a disable signal which automatically disconnects the particular functional module chosen from its actuators and displays. This disable signal is also sent to all the other functional modules as an input. Through their programs the appropriate adjustments are made in the system to compensate for the removal of the malfunctioning functional module from the system.

If the navigation computer were out, for example, the attack computer might take on a limited form of navigation. Notice that with the high computing speeds of the functional modules using the block oriented computer organization it should not be necessary to drop any system operation. Only the memory capacity might dictate that the failure mode of operation would

not be as sophisticated as the original mode. In any event, the only function to be downgraded would be that of the failed module and not necessarily that of the working functional module which has taken over the extra operation.

The STU logical structure reflects the simplicity of its responsibility. Since it must only detect and store data concerning the operating status of the functional modules, and since the modules themselves are programmable, such detection can be reduced to simple proportions. One method which might be used is the following: Each functional module will process a given group of data including selected input quantities. This manipulation would use, in different subroutines, all the elements within the array at one time or another. The result of the computation would be a test word. All functional modules would develop the same test word, provided they all were operating correctly. The test words would come to the STU bit-serial, word-parallel. If any functional module disagreed with the others, this fact would be detected through the use of a very simple serial disagreement detection logic.

Such errors when detected, would be recorded in a current status word. This word, as mentioned earlier, is sent to the pilot. It would also be sent to all the functional modules to be counted. This is done to store a count intermittent errors. These would cause only a flicker on the pilot display unless re-enforced by some means. Since all the functional modules would obtain the same test status word, they would all arrive at the conclusion that one of their members was at fault. This would be communicated to the STU which would again reach a conclusion based upon a majority statement: all the status words from the individual functional modules would be used to form a majority status word in which the failed module (or modules) would be indicated by a 1 (or 1's) in specific position in the word.

This permanent status word would be stored in the functional module in a suitable form of permanent memory which would not be affected by power transients. The output of this permanent status record would be available to the pilot on the same lines which indicate individual disagreements between the test words coming from the functional modules.

As a result of the discussion just concluded, the simplicity of the STU can be appreciated. Its MTBF even without redundancy would be high. With redundancy, failures in the STU would be reduced to the insignificant level.

Performance Considerations

Either the bi-polar or MOS transistor can be used to fabricate the arithmetic elements. If the bi-polar approach is used, higher clock rates and hence improved performance would result. For the purpose of this discussion, a 500-kc clock rate will be considered. This rate is reasonable with MOS units. A word length of 25 bits will be used. The word time of the system would then be 50 microseconds. If the blocks are operated as DDA integrators the iteration rate would be 20,000 per second.

In general, for a 25-bit word length, a total of 25 word times are required to complete the multiplications, divisions, etc, giving a total time of $25 \times 50 = 1250$ microseconds or 1.25 milliseconds for the complete operation. During this time a total of 100 multiplications would be able to be performed. This can be compared to the equivalent conventional computing speed required to complete 100 multiplications in 1.25 milliseconds. The equivalent time would be 12.5 microseconds for either a multiplication, division, or square root. Since this is based upon a 500 kc clock rate, it can be appreciated that with higher clock rates as might be possible with bi-polar transistors, a much faster multiplication would result. For example, a five-megacycle clock rate would give a 1.25 microsecond multiply. Such a speed is an order of magnitude faster than anything attainable with conventional computer organizations even though they require much more equipment than the simple 4×25 arithmetic array used in the block-oriented computer. With larger arrays, faster speeds would be possible.

In addition to the above speeds concerning the long operations of multiplication, division, etc, an average of four additions or subtractions per long operation can be performed concurrently. Thus, these short operations require no computing time and are done within the arithmetic array at the same time as the long operations.

To the time to complete the 100 long operations must be added the time to access information from the memory. The arithmetic blocks have an active program memory within themselves. However, in order to use the arithmetic blocks for more than one operation, different programs and initial constants must be supplied from an external memory. Its exact nature is unimportant, but only a read operation is required. Such read-only memories can be quite fast and should be able to accommodate bi-polar as well as MOS clock speeds.

Reliability Apraisal

Extensive reliability data is not yet available on large scale monolithic arrays. Preliminary indications are that the actual number of "transistors in a given chip is not significant in the overall failure rate of the device, and that the primary failure mechanisms are the lead connections between individual chips and multilayer wiring board or interconnection failures at the system level.

If the failure rate on the large array devices approaches that currently obtainable in present integrated circuits, a significant improvement in the system reliability would result. Current failure rates are at the 0.1 per million hours level for integrated circuits. Based on this failure rate, the 100 chip array would have a failure rate of 10 per million hours or a calculated MTBF of 100,000 hours.

When this failure rate is compared to an existing arithmetic and control unit of whatever capacity, the clear superiority in reliability is evident. Current arithmetic and control units with $30\mu s$ multiply time typically have approximately 1500 integrated circuits with a calculated MTBF of 7000 hours based on the 107 circuit BTBF.

With new memory techniques, it may be possible to obtain MTBF's to compare with that obtainable with the monolithic arrays in the arithmetic and control sections of the machine. New semiconductor memories show promise in this direction. If an equivalent improvement takes place in the memory technology, a function module with a 50,000 hour MTBF without redundancy would be possible.

2.3.9 Summary And Conclusions

The catastrophic failure mode and lack of growth capability of the centralized digital processor has long indicated a need for new logical organizations for real time systems, such as avionics. Two possible organizations have been discussed herein, the redundant and the functional modular, with the latter favored for avionics applications. The impact of new microelectronic developments is also discussed from the standpoint of applicability to the new computer organizations. Four possible logical organizations of the central processing unit have been presented, together with comparisons. It is concluded that the logical structure

should be "block oriented" to exploit the advantages of the coming generation of super chips. This implies the use of highly repetitive logic structures on the chip and the minimization of input-output lead requirements through serial or quasi-serial computation.

2.4 ANALOG-TO-DIGITAL CONVERSION

2.4.1 General

The digital computer presents the avionic system designer with a computing means which, theoretically, can be made accurate to any desired number of places. The input data to the computer, however, is typically generated by analog sensing elements, and the outputs must be used to effect control, again requiring analog signals. Thus, the overall system computing accuracy can be no greater than the basic analog-digital conversion accuracy. Analog-digital conversion is accuracy limited by the same considerations which are encountered in pure analog computers, i.e. drift, harmonics, noise, linearity, etc.

Selection of the optimum analog-to-digital and digital-to-analog interface is one of the most critical areas in aerospace computer subsystems. Not only is the conversion accuracy of primary concern, but other major constraints are encountered including weight, volume, environment, reliability, and maintainability. Quite often, the interface conversion units, multiplexers, and data buffers occupy as much volume and consume as much power as the remainder of the digital computer subsystem. With respect to reliability and maintainability, the impact of the conversion system on the overall avionics effectiveness is as critical as the digital computer subsystem per se.

Concern for the problem of compatibility of interface between subsystems will eventually lead to the establishment of standardized input-output requirements for aerospace guidance computers. Such a standardization must, of course, take into account expected advances in such areas as conversion systems, digital computer circuit and packaging, and digital computer system organization. One ameliorating factor is the increasing trend toward digital techniques in such areas as radar navigation, air data, etc. This would eliminate the need for conversion, thereby greatly simplifying the interface.

2.4.2 Typical System-Interface Requirements

Interface requirements for three different configurations are shown in Tables II-5, II-6, and II-7. The tables show only the format of interface signals for each of the subsystems. Accuracies have been deleted to avoid classification of the tables.

TABLE II-5
CENTRALIZED BOMBING/NAVIGATION SYSTEM

Interfacing Subsystem	Numbers of Independent Signal Channels									
	To Bomb Nav Sys					From Bomb/Nav				
	Synchro	ac	dc	Digital	Increment	Synchro	ac	dc	Digital	Increment
Inertial Reference Unit	2				3	2*				3
Aux Ref System	1	1								
Doppler				1	2					
Loran				3						2
Flight Control System						1				
Display Element									6	
Aided Visual Element		1		1		4		3	10	
Pilots Instruments	1					8		1		
Moving Map						2				
Attack Radar	2	2		2		3	2	1		
Terrain Follow Radar						2				
Air Data Computer	2		1							
Penetration and Warning		2				1		1		
A-G Missile	3		3			1			5	5
A-A Missile	9	7	7				16	10		
TOTALS	20	11	11	7	5	22	18	15	21	10

*Roll and Pitch Direct from IRU

TABLE II-6
ADVANCED TRANSPORT
(PRIMARY AND AUXILIARY NAVIGATION SYSTEMS)

Interfacing Subsystem	Numbers of Independent Signal Channels													
	To Prim Nav Sys					From Prim Nav Sys					To Aux Nav Sys			
	Synchro	AC	DC	Digital	Encoder	Incremental	Synchro	Sync/Geneva	AC	DC	Digital	Incremental	Synchro	Sync/Geneva
IRU (Nav Sys)	3					3	2*						2*	
Aux. Ref.	1										3		1	
Doppler					1	2							1	2
Loran				3							2			
Tacan	1		1											
VOR	1													
MM Radar				1						2				2
CADC	2	1									2	1		
Instruments							4	1	2				2	1
Malf. Det. Sys.				1						1				1
Crash Recorder										1				1
Throttle Command										4				
TOTALS	8	1	1	5	1	5	4	1	-	2	8	8	4	1

TABLE II-7
ATTACK SYSTEM - NAVIGATION SYSTEM (DUAL)

Interfacing Subsystem	Numbers of Independent Signal Channels																	
	Weapon Delivery System						Navigation System											
	To WD System			From WD System			To Nav Sys			From Nav System								
	Synchro	AC	DC	Digital	Encoder	Increment	Synchro	AC	DC	Digital	Encoder	Increment	Synchro	AC	DC	Digital	Encoder	Increment
SIRU (Nav Sys)	2					3							2*					3
Aux Rel System	1	1											1	1				
Doppler					1	2											1	2
Loran																	3	
Tacan																1	1	
Display Element											6							
Aided Visual Element							4		3	10								
Pilots Instruments							3		1						8		1	
Moving Map															2			
Attack Radar	2	2		2			3	2	1				2		3	2	1	
TFR							2								2			
CADC	2		1										2		1			
A-G Missile	3		3				1			10	10							
Penetration and Warning			2				1		1				2		1		1	
TOTALS	10	5	4	3	-	5	14	2	6	26	13	5	5	1	4	2	2	5

Table II-5 relates to the Litton ASQ-61 (A-6A) Centralized Bombing/Navigation System and is also representative of an advanced F-111 category. Table II-6 represents a dual system for the C-5 class of transports with doppler navigation and multiple fix modes. An auxiliary system can provide horizontal steering. Table II-7 represents a typical dual weapon system as might be applied to a B-52 or B-111. For this configuration it is assumed that a backup doppler-inertial navigation computation capability exists in the weapon delivery system.

A typical interface block diagram for an avionic system is shown in Figure 2-63. A listing of the signals, together with their system characteristics is given in Table II-8.

Analysis of the system input and output requirements shows that they may be separated into three classes depending on the data rates and signal conversion requirements of the transmitted data. This is shown in Figure 2-64. The first class represents the slow, near static, or discrete input-output class. The second class is represented by slowly changing data that require conversion from or to digital data. The third class is the high-data-rate information that is received or transmitted in high-frequency bursts. It is the goal of the system designer to accommodate these classes of input-output signals with a minimum of hardware and at the same time stay ahead of the system data rates so that no data are lost. Hardware reductions can be made by designing interface units within common classes to accommodate several input or output signals on a time-shared basis.

The first class of data may be controlled directly by the processor through direct communication with its accumulator. The accumulator may be connected to an input-output bus. This bus connects to all discrete inputs such as switches, input registers, etc., and to all discrete output registers. Decode logic, which receives address lines from the central processor at each discrete unit, controls bus switching. Line drivers and line receivers for signal level conversion are connected to the output and input data lines.

The second class includes digital-to-analog, analog-to-digital, encoder inputs, and code conversion input-output data. The analog signals may be ac, synchro, or dc; the encoder inputs may be a Gray code, and a BCD-to-binary or binary-to-BCD conversion for display purposes may be required. Previous to the advent of the distributed computer complex

TABLE II-8
TYPICAL INTERFACE CONFIGURATION

	SIGNAL DATA IDENTITY			MAXIMUM DATA LIMITS			
	From/ To Nav. Set	Signal Name	Type	Range	Signal Accuracy	Fraction of Full Scale	Remarks
TF Radar	From	Bearing	Digital*	360°	0.5°	10 bits	
		Drift	Digital*	±45°	0.25°	8 bits	
		Pitch	Synchro	±40°	6 minutes		
		Roll	Synchro	±80°	6 minutes		
		Groundspeed	Digital*	1000 knots	2 knots	10 bits	
		Inertial Angle of Attack	Digital*	90°	0.5°	8 bits	
AFCS	From	Steering error	Digital*	180°	0.25°	10 bits	
		Crosstrack error	Digital*	10; 100 mi	0.002; 0.02 mi.	13 bits	
Flight Director	From	Steering error	Digital*	180°	0.25°	10 bits	
		Crosstrack error	Digital*	10; 100 mi.	0.002; 0.02 mi.	13 bits	
		Range	Digital*	100; 1000; 10,000 mi.	0.02; 0.2; 2.0 mi.	13 bits	
Vertical Speed Display	From	Vertical Velocity	Digital*	5000 ft/min	3 ft/sec	8 bits	
Inertial Unit	From	Pitch	Synchro	±40°	6 minutes	10 bits	
		Roll	Synchro	±180°	6 minutes	12 bits	
		Heading	Synchro	360°	3 minutes	13 bits	
		Ground Velocity - N		1000 knots			
		Ground Velocity - E	Pulse Train	1000 knots	0.4 FPS per pulse		
		Vertical Velocity - Z		5000 ft/min			
Air Data Computer	To	True Air Speed	Digital*	600 knots	0.5 knots	11 bits	
	To	Barometric Alt.	Digital*	40,000 ft.	1.0 feet	18 bits	
Attitude & Heading Ref.	From	Ground Velocity - N	Digital*	1000 knots	3 ft/sec	9 bits	
	From	Ground Velocity - E	Digital*	1000 knots	3 ft/sec	9 bits	
	To	Pitch	Synchro	±40°	6 minutes	1/400	
	To	Roll	Synchro	±80°	6 minutes	1/600	
	To	Heading	Digital*	360°	3 minutes	14 bits	
LORAN	To	Time Difference Address Bus	Digital Discrete			19 2 states	Defines whether A or B time difference Tells whether A or B envelope has jumped ±10 mtr. per second
	To	A+	Discrete			2 states	
	To	A-	Discrete			2 states	
	To	B+	Discrete			2 states	
	To	B-	Discrete			2 states	
TACAN	To	Range	Digital	204.8 nm	0.0125 mi.	14 bits	Digital/Digital
	To	Bearing	Digital	360°	0.25°	11 bits	
Search Radar	To	Range	Digital	30 miles	10 feet	15 bits	
	To	Bearing	Digital*	180°	3 minutes	14 bits	
	From	Range Cueing	Digital*	100; 1000; 10,000 mi.	0.02; 0.2; 2.0 mi.	14 bits	
	From	Bearing Cueing	Digital*	360°	3 minutes	14 bits	
	From	Pitch	Synchro	±10°	6 minutes	1/400	
	From	Roll	Synchro	±60°	6 minutes	1/600	
	From	Heading	Synchro (2 speed)	360°	3 minutes	1/8000	
Radar Alt	To	Altitude	Digital	57,000 feet	1 foot below 5000 ft altitude	13 bits	

concept the system designer multiplexed all of these signals into a group. This facilitated conversion with a common network, one at a time, in a sequence-controlled manner. However, this scheme suffers from the same defect as the central computer - a single failure causes the entire system to be down. Thus, the necessity exists for the conversion system to be distributed also with a separate A-D converter allocated to each principal sensor or effector.

The third class of data communication may be simultaneously buffered into the computer's memory while the processor is busy executing its programs. Thus the processor is not slowed frequently to control high-data-rate transfers. The processor controls this communication with specially stored control words. The interface units control these transfers to and from the memory and have the ability to address the memory on a priority demand basis. A computer system that is designed for real time control of external events can facilitate this control with an automatic interrupt scheme. The selection of particular interrupt technique is a tradeoff of complexity vs response time requirements and programming convenience.

2.4.3 Present-Day Conversion Techniques

Data and control signals transmitted to and from the computer almost always have to be converted from analog-to-digital or from digital-to-analog form. Although there exists a great variety of types of inputs and outputs, they essentially all can be categorized as being either mechanical shaft angles or electrical quantities. Electromechanical conversion techniques may be used to convert either signal form whereas electronic converters operate only with electrical signals. The following paragraphs describe the types of electromechanical and electronic converters being used today and detail some of their performance characteristics.

Electromechanical Conversion

Analog-to-digital conversion including synchro-to-digital and dc-to-digital may be performed utilizing electromechanical servo techniques. Figure 2-65 illustrates conceptually a typical synchro-to-digital converter. The input lines from the remote synchro transmitter are connected to the control transformer whose secondary delivers an input error signal to the servo amplifier. The polarity and amplitude of this

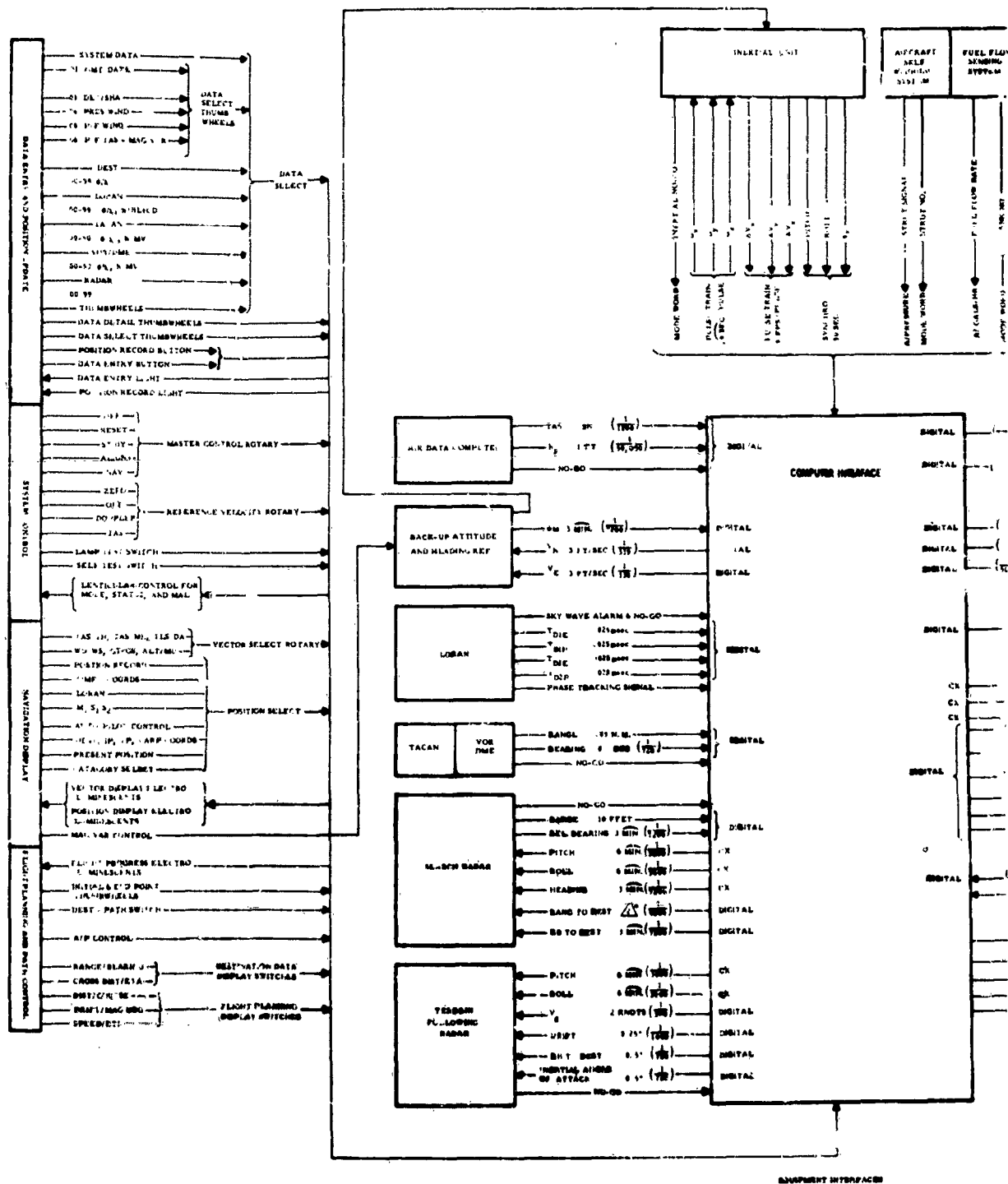
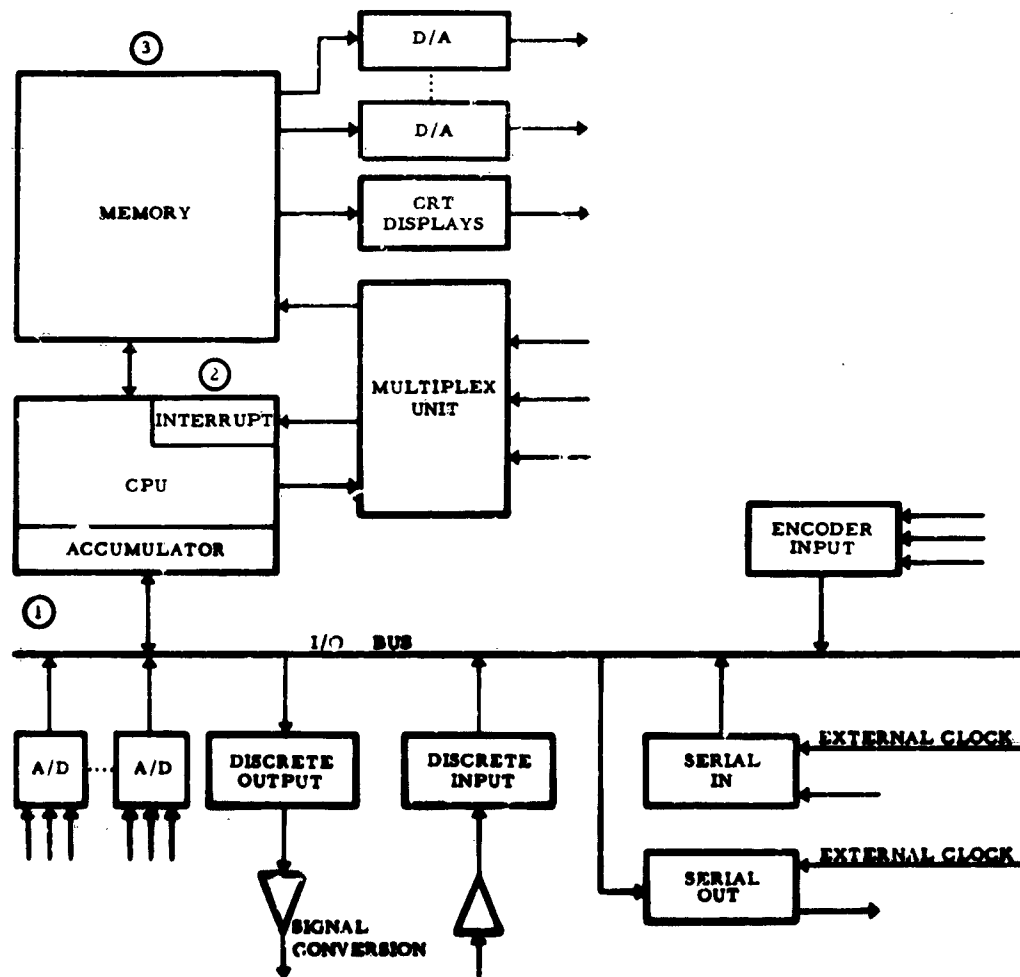


Figure 2-63. Possible Interface



ST00-190

Figure 2-64. Methods of Satisfying a Variety of Interface Requirements

error signal determines the speed and direction of the servo motor rotation. The motor drives the rotor of the control transformer, via a suitable gear train, to such a position that the rotor winding is in spatial quadrature with the net effective primary flux vector, i. e., such that the amplifier input is zero. A shaft encoder, suitably geared to the motor, is used to digitize the effective shaft position of the control transformer.

A quite similar technique, Figure 2-66, is used to digitize a dc input. In this case, however, a potentiometer is substituted for the control transformer, and the error input to the servo amplifier is derived by chopping at a 400-cps rate between the potentiometer voltage and the input voltage being digitized. For the case where the input voltage being digitized is derived from a remote potentiometer, it is desirable for both the source potentiometer and the local potentiometer to be excited from the same voltage source. This configuration relaxes the requirements of the high-precision voltage source, since variations in the voltage source tend to reflect equally on both potentiometer wipers, so that the ratio settings remain constant.

1. Shaft Angle Encoders

Digital-to-synchro conversion is normally accomplished with the use of a digital servo, as indicated in Figure 2-67. The output synchro transmitter is driven, through suitable gearing, to the desired position by a motor. A shaft encoder is used to provide position feedback information. Digital logic circuitry is used to make a comparison between the encoded shaft position and the output data being converted. The difference between the two is suitably coded and 400-cps modulated to provide an error input to the servo motor. Thus the motor is driven at a speed and in such a direction as to force the shaft position to agree, in effect, with the data to be converted. A resolver transmitter, ac potentiometer, or any other form of angle-to-analog signal transducer may be substituted for the CX.

The use of shaft angle encoders is becoming quite wide spread in military applications where direct conversion of a mechanical motion to a digital number is required. Accuracies of ± 0.01 percent (2^{13}) or ± 0.003 percent, (2^{15}) are readily available in small size encoders, with size 11 or size 18 synchro mountings. Comparable accuracies are also available in synchros or resolvers. However, to the error present in

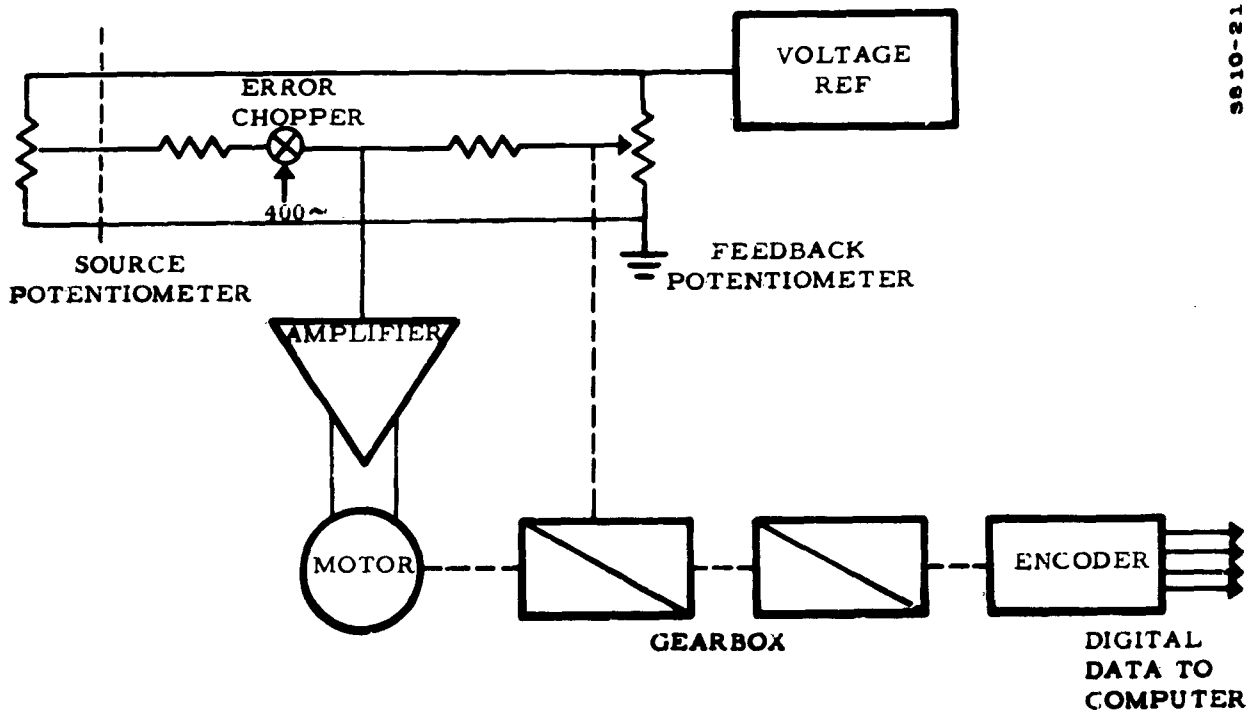


Figure 2-65. A Servo-Driven Synchro-to-Digital Converter

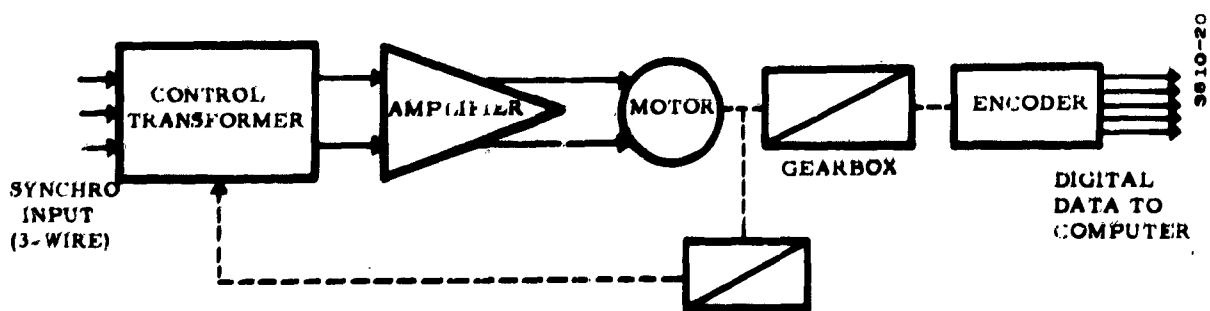


Figure 2-66. A Servo-Driven Potentiometer Analog-to-Digital Converter

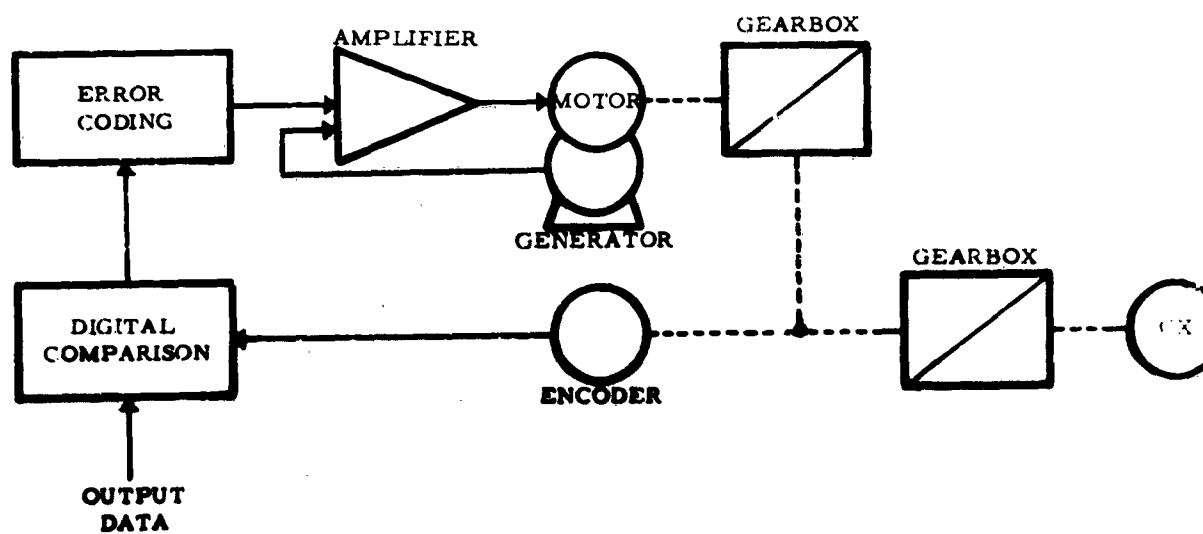


Figure 2-67. A Servo-Driven Digital-to-Synchro Converter

the synchro must be added the error contributed by the electronic converter, which also approximates ± 0.05 percent (2^{11}) to ± 0.02 percent (2^{12}) in presently available equipments. Total system error, using a synchro plus electronic conversion, therefore, may have a peak error of ± 0.1 percent (2^{10}) to ± 0.05 percent (2^{11}). Encoders are more accurate by a significant margin.

Several types of encoders are now on the market. These types are the brush or contact encoder, the newer non-contact neo-magnetic type, and the optical pickoff types. Contact type shaft encoders are now being used in a great variety of navigation and guidance equipment. The Guidance and Control Systems Division of Litton Industries is using natural binary encoders as the method of digitizing output data from its LN series inertial guidance platforms, as well as in the input/output module for the DIANE digital computer system. Some idea of the complexity involved in such a system is shown in the photo of the ASQ-61 unit Figure 2-68. This unit contains 28 shaft encoders in electromechanical servos which are used to convert remotely generated synchro signals to binary numbers for inputs and which are used in the inverse operation of generating synchro signals from binary numbers for output quantities.

2. Neo-Magnetic Encoders

For military systems, the contact type encoder will be rapidly replaced by the more reliable non-contact types. MTBF for a typical magnetic encoder supplying a 2^{13} binary output is in excess of 30,000 hours, based on conservative assignment of failure rates to the internal components. With integrated circuits, the MTBF can be raised to an excess of 75,000 hours. Life is guaranteed in excess of 200×10^6 revolutions and life expectancy should approach 1×10^9 revolutions.

Resolution and accuracy of the magnetic encoders are comparable to that obtainable in contact encoders. The presently available 2^{13} neo-magnetic encoders have a resolution of 2^8 bits per turn of the input shaft, with 32 turns of the shaft required for a full count of the encoder. Accuracy of the neo-magnetic encoders, as with the contact encoders, is ± 1 least significant bit. Therefore, accuracy of a 2^{13} encoder is ± 0.01 percent. Operating speeds of 5,000 to 10,000 rpm can be tolerated. As with all types of encoders, the neo-magnetic encoders can be supplied with a variety of code formats, such as natural binary, gray, BCD, excess 3 BCD or other special functions as may be required for system compatibility and convenience.

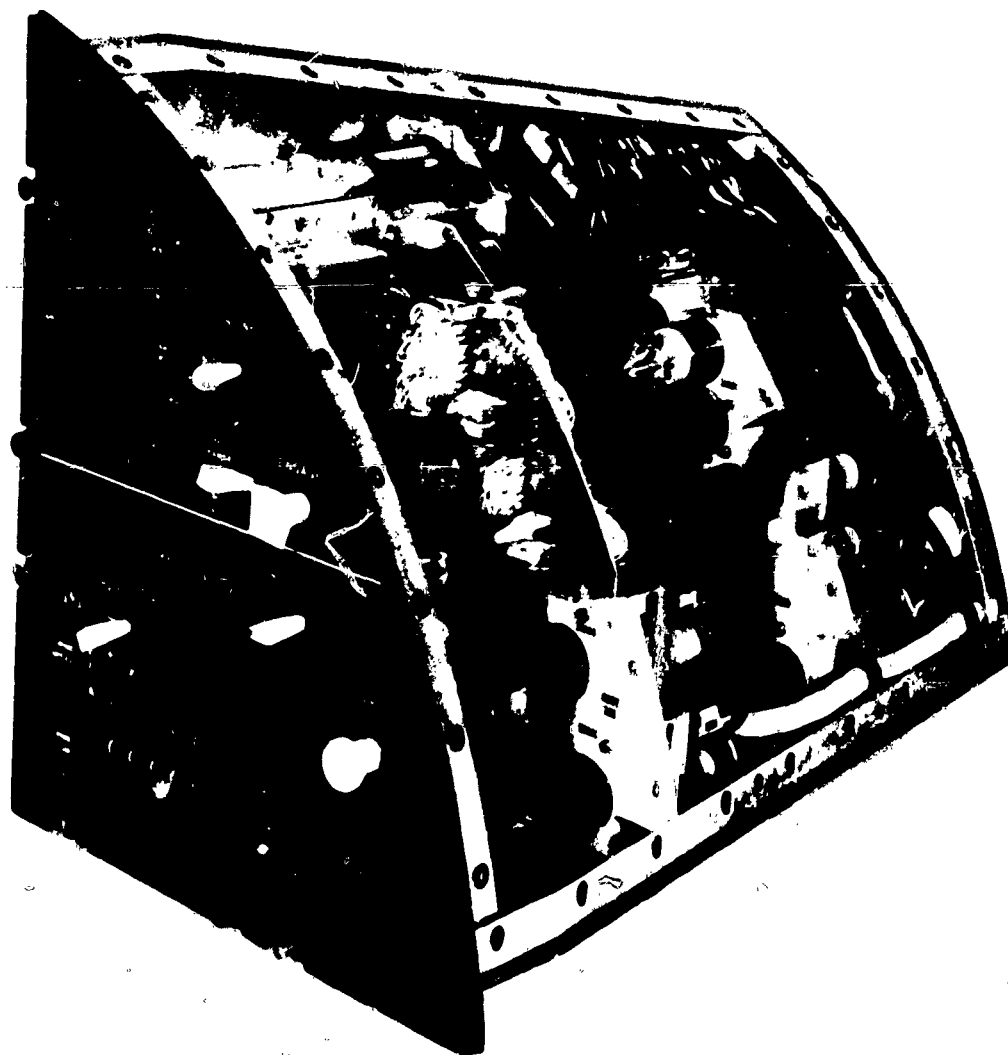


Figure 2-68. Assembly of Input-Output Shaft Encoders, ASQ-61

The neo-magnetic technique uses the permeability characteristics of an inert metallic material, and sensors are used to sense the presence or absence of these metal segments on a classic commutator disc. The new neo-magnetic encoders are not influenced by the presence of external magnetic fields and performance is not subject to possible degradation of small residual magnetic fields due to the passage of time.

Available during the last year, the neo-magnetic encoders are known to have been selected for incorporation in several new prototype navigation and guidance systems. Autonetics is using a number of 2^{13} neo-magnetic encoders for their R45 radar test program. Texas Instruments has incorporated a number of 2^{10} neo-magnetic devices into APOLLO support equipment. In addition, Lockheed has selected a 2^{14} encoder for the Mark 86 Fire Control System. In this latter application, the encoders are to operate during 70 G shock and survive 115-G shock.

At Litton, the neo-magnetic encoders are being used on a SIDS test program at Holloman, undergoing flight evaluation tests. Further, MIT is using an incremental version of the neo-magnetic encoder in their new PACE guidance system.

3. Optical Encoders

Optical encoders are available ranging from very small units 1" in diameter to extremely large and highly accurate units 8" in diameter yielding angle indication to an accuracy of one part in 2^{19} , equivalent to 2.5 seconds of arc.

In 1963, accuracy of optical encoders had reached a limit in the arc equivalent to roughly a resolution of 2^{15} in a commutator disc. The required interpolation was complex, costly and significantly decreased the reliability of the total device.

To increase the resolution available directly in a commutator disc, Litton Precision Products Division developed a special purpose pattern generating machine which, for the first time, used electron beam techniques to generate the commutator pattern. Prior to that time, radiation from visible light sources was used to generate the pattern. Since the wave length of electrons in a vacuum, such as that encountered in an electron microscope, is approximately 1/1000 that of a visible light wave, the resolution inherently available from use of electron beam techniques instead of light radiation is significantly increased.

Using the electron beam pattern generating machinery, Litton has developed the first direct reading 2^{19} optical encoder, intended for use in high accuracy navigation equipment using stellar tracking, such as the USAF SIDS system. In this device, the commutator disc contains all 19 tracks of information, and no additional electronic interpolation is required. Reliability is directly increased with this reduction in complexity.

In addition to the work on high resolution optical encoders, Litton Precision Products has pioneered development of the first solid state optical encoders, which incorporate GaAs light emitting diodes in place of the tungsten light bulbs previously used in optical devices. Use of the GaAs light sources contribute several advantages to the new encoders. Reliability and life expectancy, especially, are significantly greater than with tungsten bulb encoders. MTBF for a typical 2^{13} natural binary encoder is 35,330 hours, compared with an MTBF of 4800 hours in the same encoder using tungsten lamps.

The ability to build optical encoders in very small size in a pancake form, and the reliability available from GaAs light sources, now makes optical encoders feasible for incorporation directly onto gimbals, either in inertial platforms or radar. It is now possible to digitize gimbal position directly, without the additional cost and complexity of an external and separate analog-to-digital conversion system.

Westinghouse is proposing this type of direct gimbal to digital position encoding for a target location system in the Mark II avionics system. AC Spark Plug is proposing use of a similar device for the inertial guidance gimbals in the SRAM missile. Autonetics is proposing a similar device for both the ILAAS and Mark II versions of their R45 radar.

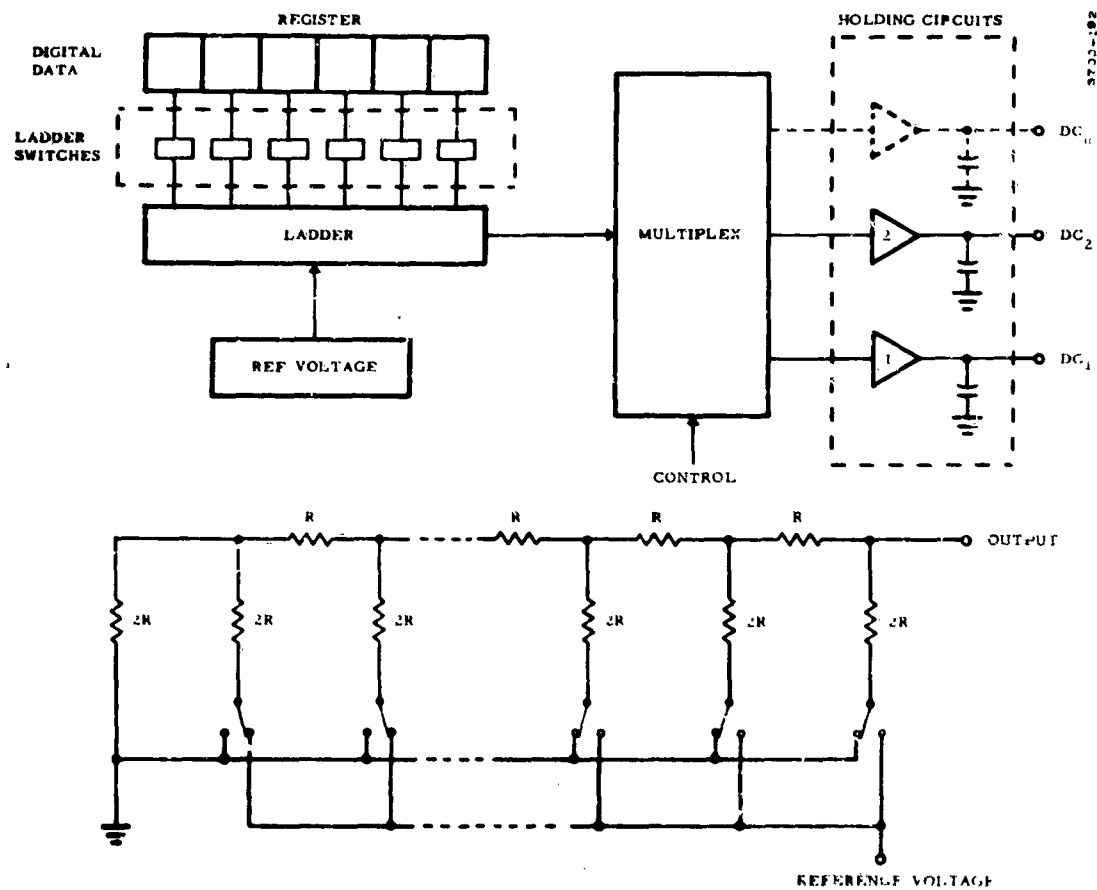
Electronic Conversion

Present day usage of electronic converters is limited primarily to the area of dc-to-digital or digital-to-dc conversion. Several electronic conversion techniques for synchro signals have been formulated and built in prototype form, but have yet to be utilized in operation systems in any significant quantity.

The virtually universal technique for electronic digital-to-analog conversion employs some form of multisection, switchable attenuation network. (See Figure 2-69.) Each digit of the number to be converted controls the setting of its associated switch so as to make a binary-weighted contribution to the network output voltage. While this approach has been characterized by about two orders of magnitude lower accuracy than that using servo techniques, factors of weight, volume, power dissipation, and reliability have motivated considerable recent development effort in electronic methods. The network technique is presently capable of about 0.05 percent accuracy for dynamic ranges in the vicinity of plus to minus 10 volts. Some degradation of this figure can be expected if power buffering is required; however, it is likely that this can be at least partially offset by further development in stable voltage standards. Conversion speed is usually more limited by input computer iteration rates than by the network itself, network response time being of the order of 2 to 10 microseconds, depending on load capacitance and network impedance.

In practical systems greater conversion hardware efficiency, as well as more efficient use of computer hardware are obtained by time-sharing of a single network among a number of analog output channels, by using some form of sample and hold, or "boxcar" technique. (With the advent of thin-film networks having the requisite accuracy but occupying much less space, it is likely that multiple networks will be used for reasons previously mentioned.) Naturally, this introduces some degradation in accuracy and bandwidth. Typical current systems of this type can achieve overall conversion accuracies in the vicinity of 0.2 percent at slew times of 0.1 to 1 second with 30 output channels. It is likely that further development extending the accuracy to the vicinity of 0.05 percent with similar slew speeds can be achieved by reducing the number of output channels. This sort of system is readily adapted to ac and synchro types of outputs by providing for suitable means of modulation and power amplification of the boxcar circuit output.

The most fundamental limitation on digital-to-analog conversion accuracy is the stability of available voltage standards suitable for airborne environment. The usual device for this purpose is the temperature-compensated Zener diode. Present units are capable of about 0.05 percent accuracy over usual military-specification temperature ranges. A second serious limitation is the departure from ideal of the binary network switches, especially the variation in saturated resistance of the



NOTE

1. Switches are symbolized. Actual units are electronic.
2. S_1 represents most significant digit; S_n least significant.
3. Bilateral operation may be obtained by substituting a negative reference voltage for ground.

Figure 2-69. A Type of Digital-to-Analog Network

transistors available for this purpose. This can be somewhat offset by choosing the basic network impedance high; however, this usually results in sacrifice of the network response time and increases the problem of accurate output power amplification. The remaining limitations are those inherent with analog operational amplifiers, especially drift, gain stability, and bandwidths.

Analog-to-Digital Conversion

There are several techniques for analog-to-digital conversion, but the most adaptable has been found to be the one commonly referred to as the method of successive approximation (Figure 2-70). It is characterized by relatively high speed, good accuracy, low hardware count, and the ability to be multiplexed to a number of input channels. In addition, it can quite easily be adapted to a number of different types of input signals. The technique consists in using a voltage comparator to make a series of weighings between the unknown input voltage and the output of a digital-to-analog network. The settings of the network are successively corrected by a set of logic rules so as to make the network output voltage converge toward the value of the voltage being converted until by the time conversion is complete, the two are arbitrarily close to one another. The network settings, as stored in a flip-flop register, form the converted output number.

Although this technique has in the past been limited in accuracy to the vicinity of 0.5 to 1 percent, recent advances have carried it to the realm of 0.1 percent over the temperature range of -55°C to 100°C with multiplexed inputs. It is expected that temperature control and further development can bring the accuracy to the area of 0.02 to 0.05 percent. Typical conversion speed for this technique runs about 5 to 10 microseconds per digit. For high accuracy, the practical limit on the number of multiplexed input channels is about 16 per conversion. Multiplexing contributes some error due to the cumulative leakage current and shunt capacitance of each multiplex switch added to the commutated mode. This technique may be used to digitize a shaft position by first converting to an analog voltage with a potentiometer.

A common candidate for digitization is the output of a synchro or resolver, and there has been a considerable amount of effort devoted to the development of electronic conversion techniques for this type of signal. Among the methods proposed, the most efficient seems to be

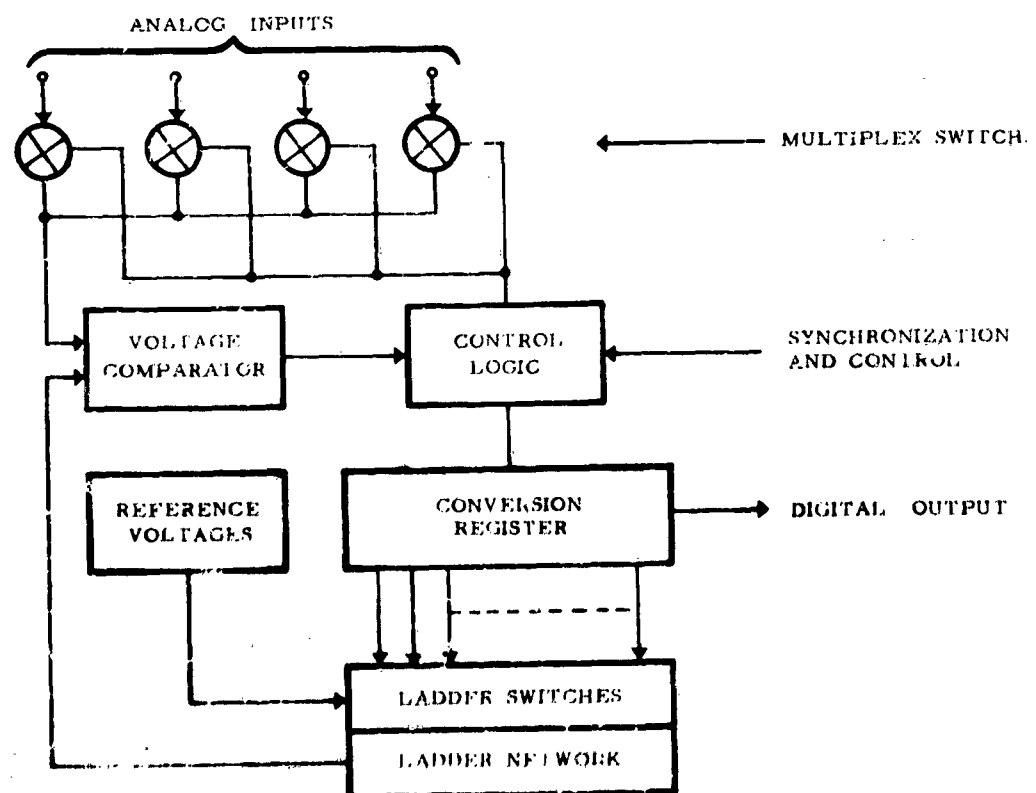


Figure 2-70. A Basic Analog-to-Digital Converter

that which basically adapts the electronic technique already described to the peculiarities of the synchro output. In this case the attenuator network may be modified to give a piecewise linear approximation to a trigonometric function, in which case digitization yields the shaft angle itself, or a pair of linear conversions may be made to yield two trigonometric functions of the shaft angle in digital form. With this latter approach it is feasible, with some restrictions, to multiplex synchro inputs intermixed with dc type inputs into the same converter.

For multiplexed synchro inputs, conversion speed resolves itself into a problem in desired data rates, since the intelligence of the signal is modulated with a relatively low-frequency carrier, and only one or two conversions can be made at a time.

Synchro-to-Digital and Digital-to-Synchro Conversion

The $\cos \theta \tan \theta'$ Multiplication Synchro-to-Digital Converter

The basic tangent multiplication system is illustrated in Figure 2-71. The synchro stator leads are applied to a pair of transformers in a Scott T connection or one transformed by solid-state methods so that the outputs are:

$$e_1 = E \sin \omega t \sin \theta$$

and

$$e_2 = E \sin \omega t \cos \theta$$

A nonlinear attenuator consisting of transformer taps, resistive dividers, or ladder networks, multiplies its input voltage by $\tan \theta'$ so that

$$e_3 = E \sin \omega t \cos \theta \tan \theta'$$

By taking the difference $e_1 - e_3$, demodulating, and applying to a Schmitt Trigger circuit, a logic signal is obtained which drives the θ' register (in serial steps) until

$$e_1 = e_3.$$

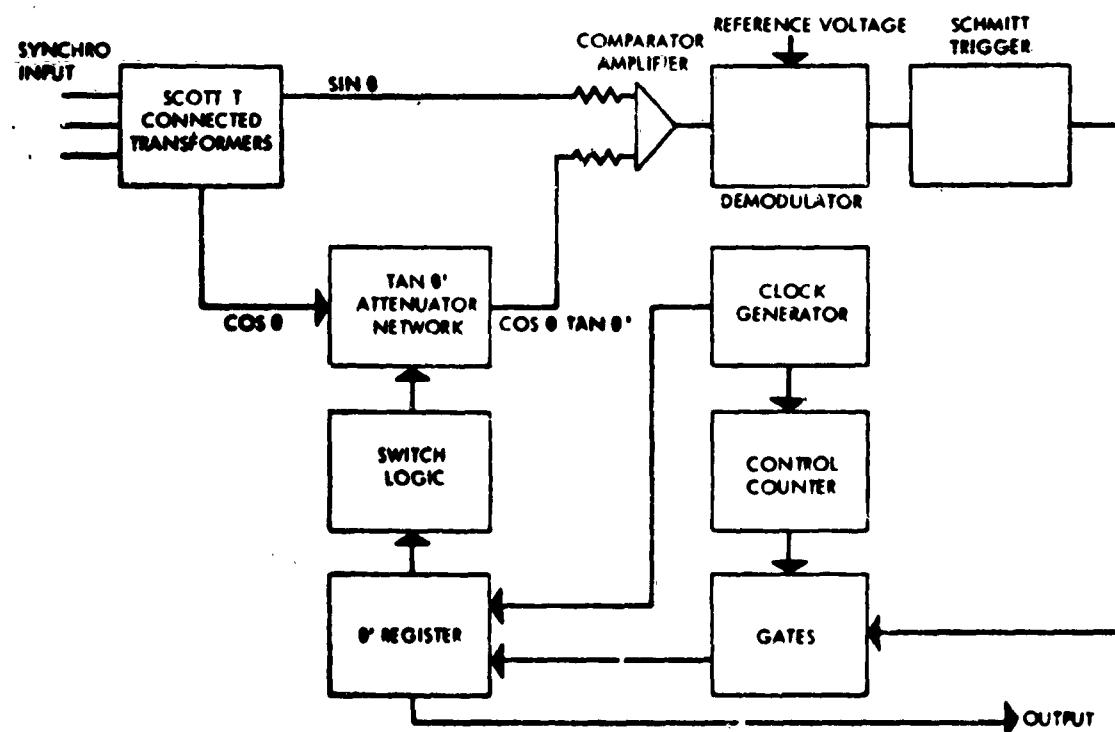


Figure 2-71. $\cos\theta \tan\theta$ Multiplication Synchro-to-Digital Converter

Then

$$E \sin \omega t \sin \theta = E \sin \omega t \cos \theta \tan \theta'$$

$$\tan \theta = \tan \theta'$$

and

$$\theta = \theta'$$

While this technique requires the use of only one attenuator network, two difficulties are encountered which offset this advantage:

1. Between $\theta = 45^\circ$ and 90° , the value of $\tan \theta$ increases from 1.0 to infinity. This difficulty may be overcome by using the cotangent function between $\theta' = 45^\circ$ and 90° . To do this requires interchanging $\sin \theta$ and $\cos \theta$, which requires extra logic and extra switches.
2. The accuracy to which the function $\tan \theta$ (or $\cotan \theta$) must be approximated is very high. The maximum error in a two-segment approximation to the $\tan \theta$ function (0 to 45°) is approximately 0.45° . The maximum error in an eight-segment approximation is approximately 0.12° .

The $\sin \theta \cos \theta' - \cos \theta \sin$ Comparison Technique

The basic $\sin \theta \cos \theta - \cos \theta \sin \theta$ comparison approach is illustrated in Figure 2-72. The synchro stator voltages

$$e_a = E \sin \omega t \sin \theta$$

$$e_b = E \sin \omega t \sin \left(\theta + \frac{2\pi}{3} \right)$$

$$e_c = E \sin \omega t \sin \left(\theta - \frac{2\pi}{3} \right)$$

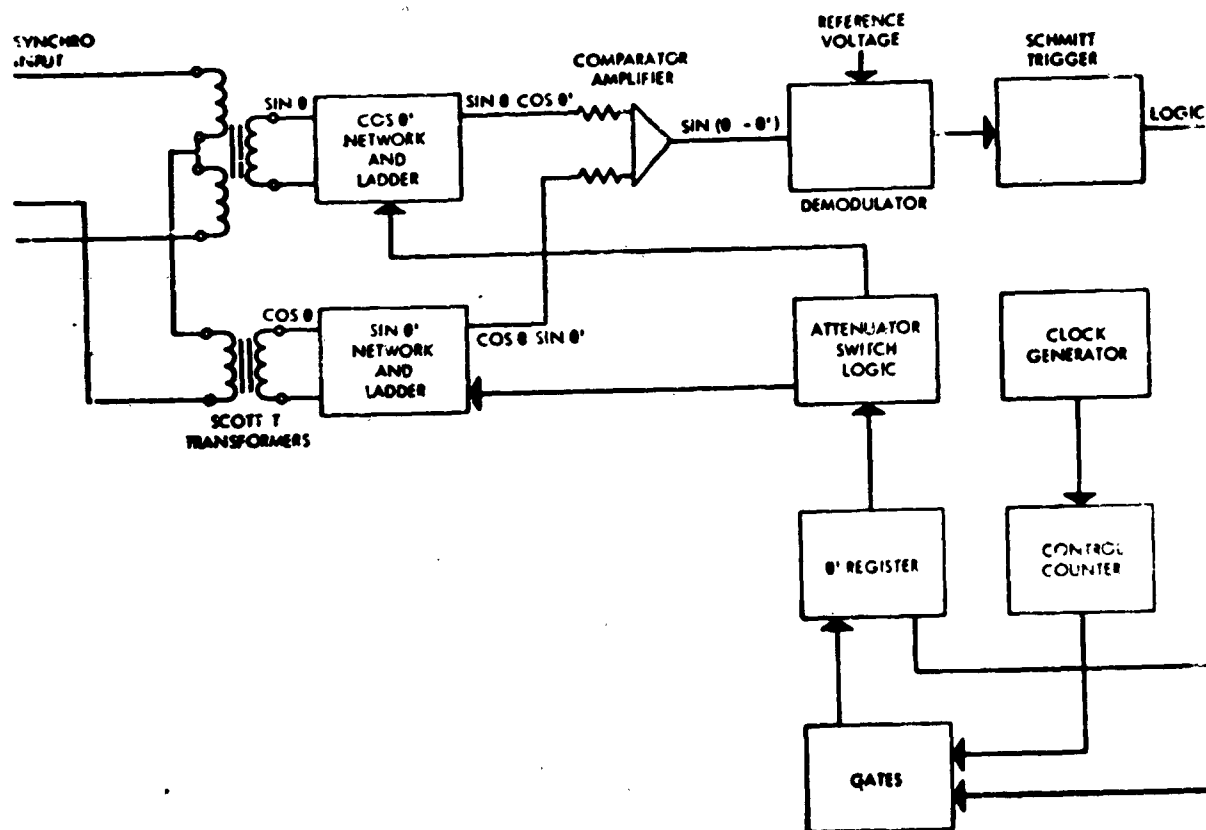


Figure 2-72. $\sin \theta \cos \theta' - \cos \theta \sin \theta'$ Comparison

are converted to

$$e_1 = E \sin \omega t \sin \theta$$

$$e_2 = E \sin \omega t \cos \theta$$

by utilizing a Scott T transformer connection. Two attenuator networks composed of resistive dividers (or taps on the transformer secondary windings) and resistor ladder networks multiply e_1 and e_2 by $\cos \theta'$ and $\sin \theta'$ respectively

The switches in the two attenuator networks are driven by the θ' register, which is composed of flip-flops or other memory elements. Two attenuators are identical but slight differences in the switch logic account for the fact that one generates the function $\sin \theta'$ while the other generates the function $\cos \theta'$.

As indicated in Figure 2-72, the output from the two networks are

$$E \sin \omega t \sin \theta \cos \theta'$$

and

$$E \sin \omega t \cos \theta \sin \theta'.$$

These signals are applied to the comparator amplifier so that its output is

$$E \sin (\theta - \theta').$$

This error signal is demodulated and applied to a Schmitt Trigger circuit, the output of which is a logic signal dependent on the polarity of the error signal.

The logic signal at the output of the Schmitt Trigger circuit causes the θ' register to increase or decrease until θ is equal to θ' . To do this, the θ' register is initially set at

1 0 0 0 0 0 0 0

and a comparison made. If the error is positive, the register is set at

0 1 0 0 0 0 0 0

and another comparison made. If the error is negative, the register is set at

1 1 0 0 0 0 0 0

and another comparison made. By continuing this process until all elements in the register have been set by a comparison, the angle θ is obtained as the state of the register (limited by the accuracy and resolution of the system).

The two outstanding advantages of this technique are:

- The same hardware used in digital-to-synchro conversion may also be used in synchro-to-digital conversion. This allows a significant standardization or use of building blocks. In some systems the digital-to-synchro and synchro-to-digital conversion may not occur simultaneously and the converter and channel may be time shared.
- Because the approximations of $\sin \theta'$ and $\cos \theta'$ are identical (straight line segments), the errors in the approximation tend to cancel. This results in a higher accuracy for a given number of network components (or fewer total network components for a given accuracy).

The Multiple Comparison Synchro-to-Digital Converter

A proven method for performing the synchro-to-digital conversion is illustrated in Figure 2-73. A Scott-T transformer connection accepts the three Synchro Transmitter Stator signals:

$$e_a = E \sin \omega t \sin \theta$$

$$e_b = E \sin \omega t \sin \left(\theta + \frac{2\pi}{3} \right)$$

$$e_c = E \sin \omega t \sin \left(\theta - \frac{2\pi}{3} \right)$$

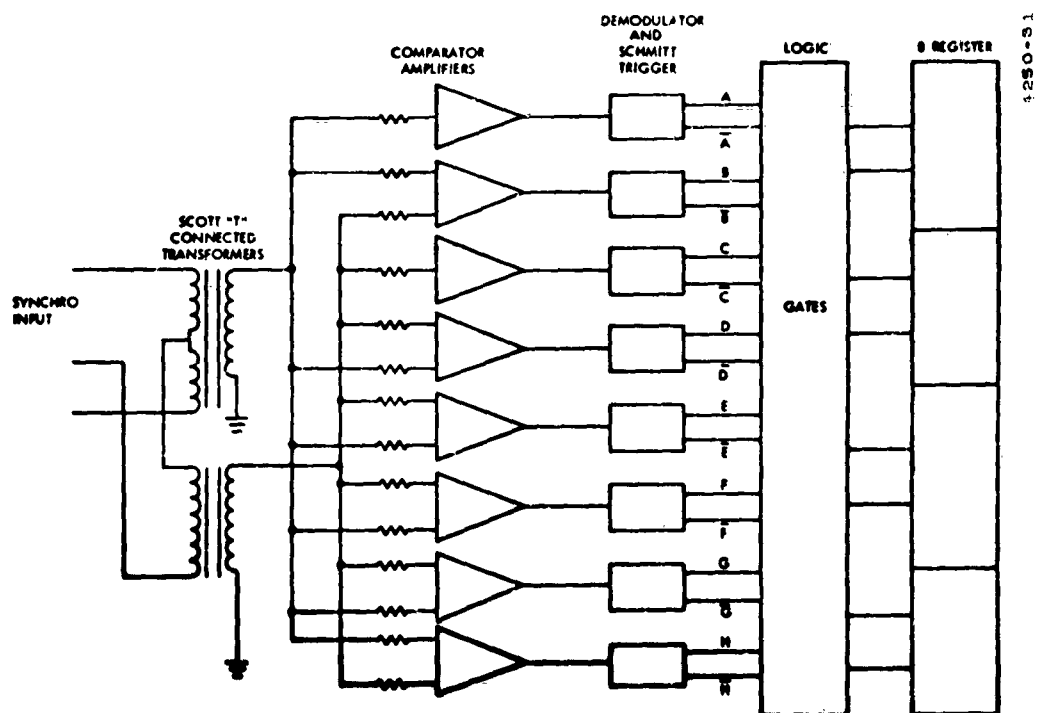


Figure 2-73. Multiple Comparison Synchro-to-Digital Converter

and by the process of vector addition, furnishes the two signals

$$e_1 = E_1 \sin \omega t \sin \theta$$

$$e_2 = E_1 \sin \omega t \cos \theta$$

at the secondary windings of the two transformers.

The two secondary windings of the transformers are connected to eight "logic" comparators, each consisting of an ac summing amplifier, a demodulator, and a Schmitt Trigger circuit. Values of amplifier summing resistors are selected so that a new vector is formed at the input to each amplifier. Vectors (or voltages that are zero with a positive slope) are formed at 0°, 45°, 90°, etc., at 45 degree intervals.

If the logic quantity A is denoted as the condition that the first vector is negative, then the most significant digit of the binary number for the angle is

$$\text{MSD} = A,$$

since the vector will be positive for the first 180 degrees and negative for the second 180 degrees. In a similar manner, logic expressions may be determined for the four most significant digits of the angle. The logic equation for the fourth most significant digit of the angle is

$$4 \text{ MSD} = \overline{A}H + \overline{A}H + BE + \overline{B}\overline{E} + CF + \overline{C}\overline{F} + DG + \overline{D}\overline{G}$$

where the letters B to H represent vectors at the remaining angles.

An inspection of the multiple comparison method for synchro-to-digital conversion will reveal that the technique may be used to perform a serial conversion, a parallel conversion, or a serial-parallel conversion (combination of serial and parallel).

A parallel conversion using this method is very attractive if only a few digits of resolution are desired. The complete conversion takes place in one clock time. However, it may be shown that:

Two comparators and 6 gates are required for the 2nd digit.

Four comparators and 12 gates are required for the 3rd digit.

Eight comparators and 24 gates are required for the 4th digit.

Sixteen comparators and 48 gates are required for the 5th digit.

2^{N-1} comparators and $3 \times 2^{N-1}$ gates are required for the Nth digit.

Therefore, for an eleven-digit conversion, 512 comparators and 1536 gates are required to solve the logic equation for the eleventh digit. A total of 3066 gates are necessary to obtain all eleven digits. It is obvious that a purely parallel converter for a resolution of more than five or six digits would very rarely be practical.

A serial or sequential converter could of course be implemented with this technique. A single comparator would be sequentially switched to appropriate transformer taps to obtain the proper binary number. Connection to proper transformer taps would be determined by logic equations (dependent on values obtained for the more significant digits).

There is little doubt that the most useful application of the multiple comparison converter principle is in a serial-parallel arrangement. A very fast conversion can be accomplished by making a compromise between the number of comparators required and the number of required serial steps. For example, by using 32 comparators, the six most significant digits of the number representing the angle can be determined in one clock period. During the second clock period, a resistive network is connected between the proper segments and 31 comparators used to determine the remaining five digits. The complete eleven bit conversion therefore, would take place in two clock times - possibly less than 15 microseconds. For some system applications, this speed may be important and would justify the extra hardware required to implement it.

The Rotor Excitation Voltage Comparison Method

When the synchro excitation voltage is also available at the synchro-to-digital converter, a method of synchro-to-digital conversion may be used which will be called the Rotor Excitation Comparison Method. This is a variation of the multiple comparison method which was described previously.

Four summation amplifiers provide the four voltages e_1, e_2, e_3, e_4 and their inverse voltages e_5, e_6, e_7, e_8 , representing octant vectors as shown in Figure 2-74. These eight signals are applied to eight comparators to set the octant register (the four most significant digits of the binary number for θ).

The octant logic also closes the proper selection switch to apply the proper voltage to another comparator. The voltage applied is a linear segment between $e_1, e_2, e_3, e_4, e_5, e_6, e_7$, or e_8 , depending on what octant has been selected. This voltage is then compared with the output from a ladder which has been excited with the synchro rotor excitation voltage. A serial conversion now occurs to obtain the least significant digits of the angle θ .

This method of conversion is excellent in a system requiring very high resolution at lower accuracy. Its biggest disadvantage is the requirement that the rotor excitation voltage be available. If another load were placed on the synchro, a relatively large error would be caused by a change in amplitude ratio between rotor and stator voltages.

K sin θ , K Cos θ Synchro-to-Digital Converter

The basic K sin θ , K cos θ conversion technique is illustrated in Figure 2-75. The Scott T connected transformers convert the three synchro transmitter stator signals into the form:

$$e_1 = K \sin \omega t \sin \theta$$

$$e_2 = K \sin \omega t \cos \theta$$

The voltages are interrogated and converted at the peak amplitude of the carrier signal. Conversion is generally performed utilizing a successive approximation technique which employs a linear binary-coded ladder network to generate the comparison voltage.

The data presented to the computer is in the form of K sin θ and K cos θ . It is unnecessary, perhaps even undesirable for the converter to yield the angle itself, since more often than not, it is the trigonometric form which is used in the program computations. The constant K in the

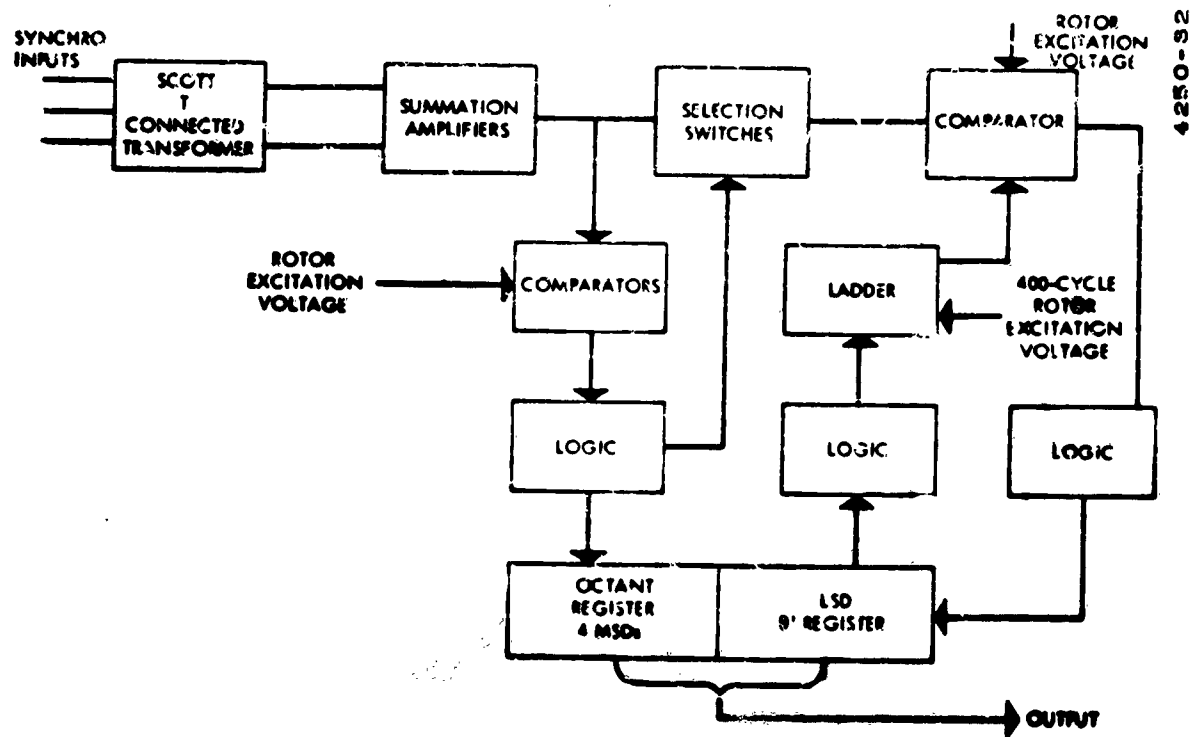


Figure 2-74. Rotor Excitation Voltage Comparison Technique

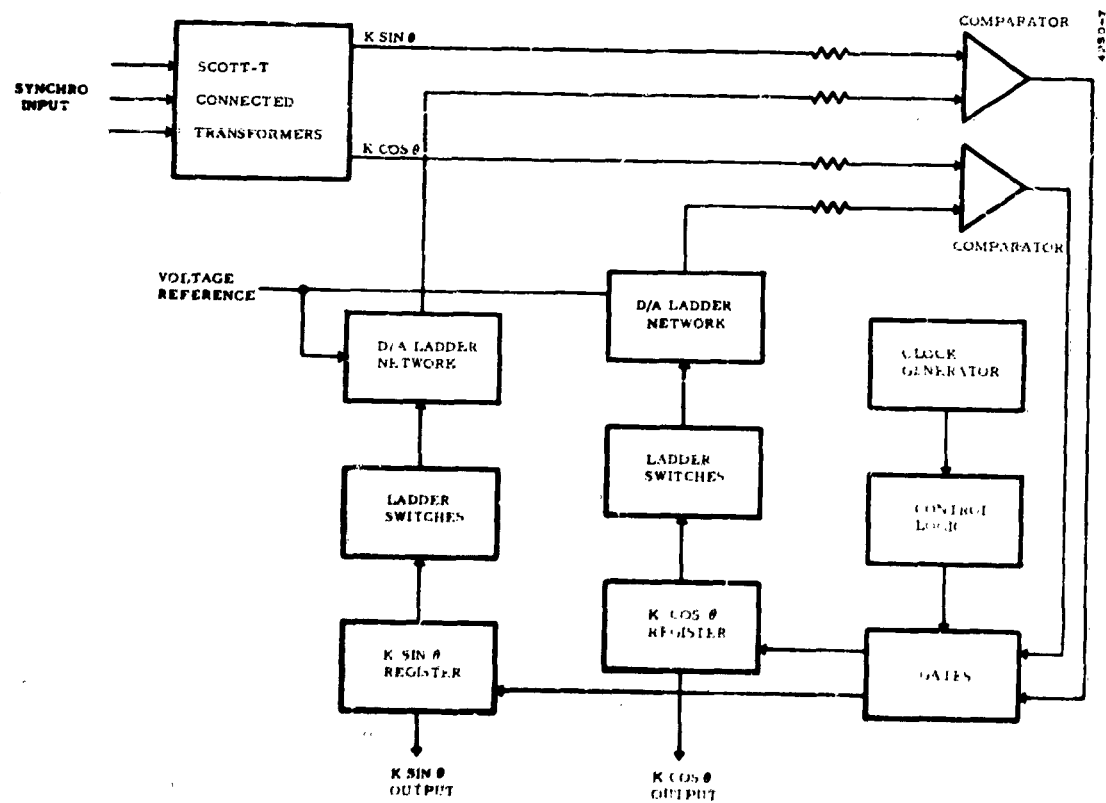


Figure 2-75. K Sin, K Cos Synchro-to-Digital Converter

expressions above is, or can be made nearly equal to unity. It is primarily a function of the turns ratio of the synchro and the turns ratio of the Scott-T transformers. It is also a function of the relative harmonic content of the voltages presented to the comparator. For purposes of accuracy, it is necessary for the computer to calculate K by taking the square root of the sum of the squares of the conversion data pair and dividing each datum by K to yield the true sine and cosine.

Digital-to-Synchro Conversion Utilizing Sine and Cosine Function Generator

The basic conversion scheme, illustrated in Figure 2-76 utilizes the sine and cosine function generators discussed earlier. The system operation consists of receiving the digital word representing the angle θ and logically driving the electronic switches of the sine and cosine function generators to produce the functions $A \sin \theta$ and $A \cos \theta$, where A is the peak voltage of the carrier. The functions are supplied to the Scott-T transformer configuration. By using the appropriate turns ratio, the following synchro signals are generated at the output

$$e_{12} = A \sin \theta$$

$$e_{23} = 1/2A (3 \cos \theta + \sin \theta)$$

$$e_{32} = -1/2A (\sin \theta + 3 \cos \theta)$$

which are equivalent to the desired outputs

$$e_{12} = A \sin \theta$$

$$e_{23} = A \sin (\theta + 120^\circ)$$

$$e_{32} = A \sin (\theta + 240^\circ)$$

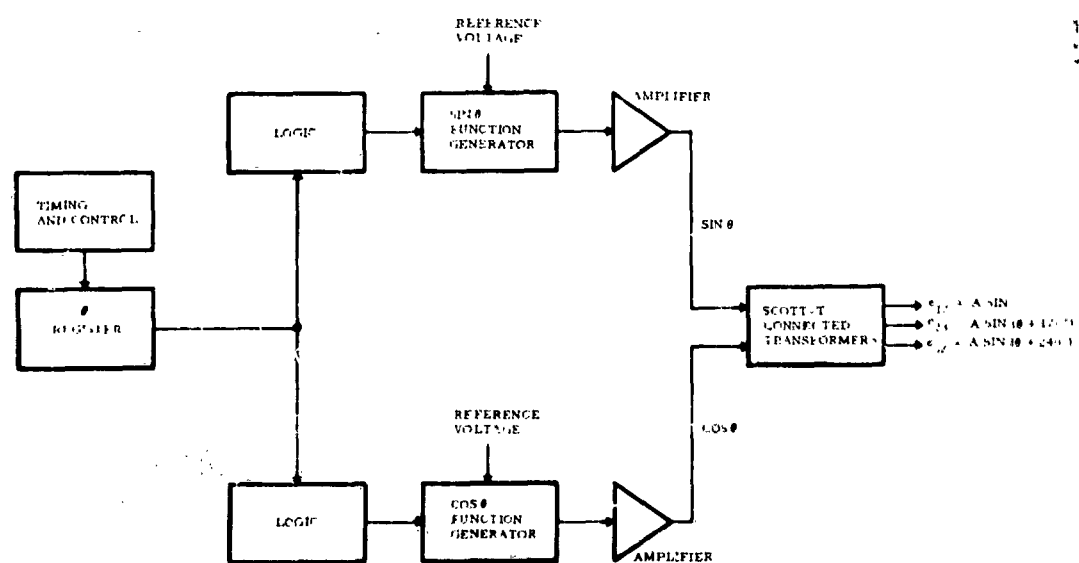


Figure 2-76. Digital-to-Synchro Converter Utilizing Sine and Cosine Function Generators

Digital-to-Synchro Conversion Utilization Sine and Cosine Modulators

Digital-to-synchro conversion is partially performed by a digital-to-dc converter which consists of a D/A voltage ladder network. Two dc output channels are used to generate a sine-cosine data pair in dc form. For convenience and accuracy, the computer supplies the sine and the cosine directly, since program computations relating to angles are generally performed in trigonometric form. This permits the use of the linear ladder network, and eliminates the use of the usual linear approximation type of approach necessary when the angle itself is given.

Additional circuitry as indicated in Figure 2-77 is used to modulate an ac reference carrier with the sine and the cosine, respectively. The modulated carrier is power amplified before delivery to the output. The power amplifier incorporates feedback with a moderate amount of frequency selection. The primary reason for the feedback is to provide as much amplitude linearity as possible, since it is the amplitude ratio of the sine-cosine signal pair which is critical in obtaining an accurate synchro position. Because of the relatively low carrier frequency and the narrow required bandwidth, the desired degree of amplitude linearity can be easily achieved.

Summary of Converter Characteristics

Of importance in system design is the available accuracy, conversion speed, and multiplex capability. Table II-9 lists these characteristics for various types of converters.

Some comments in connection with accuracy seem in order. With any conversion technique, accuracy has meaning only if some operational context is provided, such as how the signal originates, how it is used, or how the error is to be measured. All accuracies herein quoted (Table II-9) are defined as the quotient of the maximum error to the

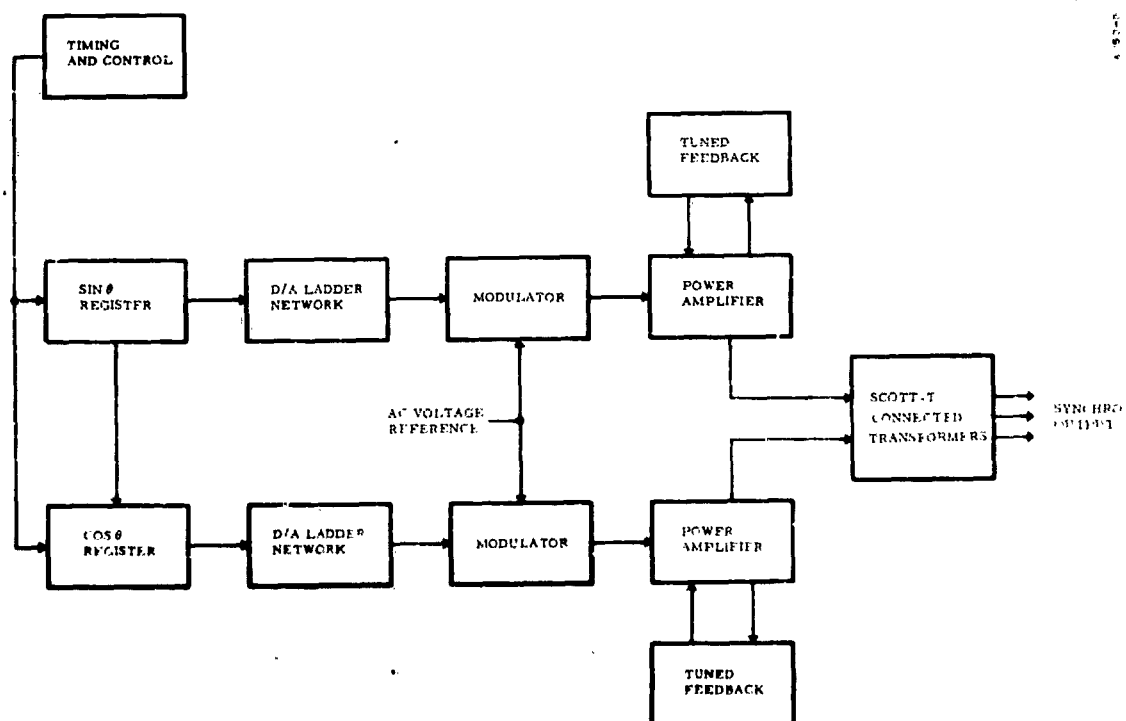


Figure 2-77. Digital-to-Synchro Converter Utilizing Sine and Cosine Modulators

TABLE II-9

CHARACTERISTICS OF VARIOUS CONVERSION TECHNIQUES

Data herein are intended to merely represent and not indicate relationships among characteristics.

Technique	Accuracy	Conversion Speed	Multiplex Channels
<u>Analog-to-Digital</u>			
Shaft Position Available			
1. Encoder, Contact	2^{12} - 2^{18}	10-100 μ sec	20-50
2. Encoder, Noncontact	2^{12} - 2^{18}	10-100 μ sec	20-50
3. Potentiometer, Electronic Converter	2^7 - 2^{10}	50-150 μ sec	10-15
4. Synchro, Electronic Converter	2^8 - 2^{12}	25,000 μ sec	8-10
Independent Voltage			
1. Electronic Converter	2^7 - 2^9	50-150 μ sec	10-15
2. Servo, Shaft Encoder	2^{10} - 2^{14}	10-100 μ sec	1
<u>Digital-to-Analog</u>			
Electronic			
1. Individual Ladder	2^7 - 2^{11}	5-20 μ sec	1
2. Multiplexed Ladder	2^6 - 2^{10}	50-1000 μ sec	10-30
3. Ladder-to-Synchro	2^8 - 2^{12}	50-1000 μ sec	5-15
Electromechanical			
1. Digital Servo	2^9 - 2^{13}	1000-15000 μ sec	1

peak-to-peak dynamic range of the variable. While this definition is quite standard, even it can lead to confusion, for instance, in the case of a shaft encoder without the further information that the dynamic range of the input is 32 turns or 11,520 arc degrees. Moreover, the accuracy of the output voltage of the servo with a potentiometer cannot be reckoned absolutely, since the servo can only control the wiper position ratio and not the excitation voltage nor the load impedance. However, such ratio accuracy is often adequate to the nature of the terminal equipment. Accuracy meanings of ac voltages are particularly difficult to interpret without some operational context since rms measurements and peak measurements are intimately bound up with harmonic content. Finally, when only absolute accuracy is appropriate, some attention must be given to the possible disparity in the respective voltage standards carried by the generating and receiving equipment.

2.4.4 Progress in New Input-Output Techniques

In connection with its work in development of digital-inertial navigation equipments, Litton has been engaged in both house-funded and contracted efforts in the development of new interfacing techniques for future systems. Some of these new concepts being looked at or already in construction are described in the following pages.

Sensor-Located Input Conversion Systems

Since analog quantities such as dc and synchro voltages are relatively sensitive to noise and also are difficult to protect using redundancy techniques, it seems desirable, from a systems viewpoint at least, to perform all conversions from analog quantities to a standardized digital from as near to the transducer as possible. Ideally, such a conversion would take place at the sensor itself.

Advances in the state-of-the-art of microelectronic integrated circuits make the construction of such things as ladder converters on single chips a distinct possibility. Such miniscule wafers having the capability of containing up to 1,000 circuit elements would combine ultra high reliability with low cost, and make practical the sensor-oriented conversion system. Even if not all of the converter (for example, the precision resistors) could be placed on the chip, the cost, size, weight, and reliability advantages would still be significant.

In this concept, each of the converters would be associated with its corresponding sensor. There would be no queuing problem normally found in large conventional systems where a single converter is time shared among many inputs. In addition to converting the analog quantity to digital form, it would also be the function of the converter to include error protection means, such as parity and complementary lines. This is done in recognition of the possibility of sensor failure and also failure of the linkage between the sensor and the central or distributed processor unit. This failure can occur in the connectors, to cite a principal source.

Direct Digital Outputting Transducers

The need for transducers that could sense a physical phenomenon and simultaneously produce a digital output indicating the magnitude of the phenomenon has become pronounced in recent years with the trend toward the universal use of digital techniques in disseminating, recording, and evaluating data. Ideally the transducer should, as an inherent feature, produce a digital signal directly from an analog input. Such a basic level concept would obviate the necessity of intermediate steps such as analog followup servo systems driving shaft encoders, voltage-to-digital converting circuitry, etc.

Three major techniques have been studied by Litton as possible solutions to the basic level transducer:

1. Natural discrete phenomena such as Brownian movement, Johnson (thermal) noise, and nuclear disintegration to name a few.
2. Frequency- or pulse-generating sensors employing piezoelectric crystals.
3. Digital force-balance deflection-generating transducers.

From all of these techniques investigated two conclusions were held in common:

1. Natural digital phenomena apparently do not exist.
2. Natural discrete and pulse phenomena represent a digital quantity only when associated with a time interval.

The discrete effects found in nature, investigated in the first technique, are random and therefore would require long sampling period or other special elaborate techniques in order to obtain the required degree of accuracy.

Both of the other techniques show great promise of providing the characteristics necessary for successful design and construction of a Digital Pressure Transducer.

In the absence of discovery of a natural phenomenon that provide a direct analog-pressure-to-digital conversion, the problem of building an instrument to perform this task may be divided into several problems corresponding to intermediate steps of conversion. For convenience (but not necessarily completeness) these might be reduced to three basic steps:

Step 1 - Hydraulic-to-mechanical conversion

Step 2 - Mechanical-to-electrical conversion

Step 3 - Binary digital encoding

Step 1 might include a pressure-to-force conversion or pressure-to-deflection conversion as provided by a diaphragm. Step 2 would include a deflection-to-resistance or-capacitance conversion or a force-to-frequency conversion as used in strain gauge sensors and piezoelectric sensors, respectively. Step 3 would include standard analog-to-digital voltage conversion, voltage-to-shaft-position conversion, and back-to-digital-voltage conversion, as well as various pulse (frequency) counting techniques.

Each step of conversion can be expected to contribute toward non-linearities, temperature sensitivity, and other errors. The selection of a particular technique must be based not only upon these factors but also upon the complexity, size and interaction of equipment required for each state of conversion.

D-A Thin-Film Ladders

Parallel D-A converters are those that simultaneously operate on each of the bits of a binary number to achieve an analog representation of that number, usually a voltage or current. Here we consider it to be a current delivered to an amplifier's summing point.

Parallel conversion (as opposed to rate multiplication conversion, discussed elsewhere) is required wherever the analog signal must be differentiated, or where the required speed of conversion precludes smoothing of the converter output. These applications usually require 6- to 10-bit resolution, appreciably less than that required by the principal components of a navigation computation. A specific application involving data wholly within a hybrid computer would be in the generation of Coriolis acceleration terms, for which the signal input to a multiplier must be ripple-free but need be known only to 0.25 percent.

Weighted resistor networks and ladder networks based on wire-wound resistors and hard contact switching have been in use for many years. The same networks, used with discrete semiconductor switching have been used recently. Accuracies generally achieved are in the 8-bit range. (See Figure 2-78.)

One area requiring reevaluation is the choice of switching methods in light of recent information as to the cost of various semiconductor devices in monolithic integrated form. It is anticipated that optimum circuits will be of different topology than their discrete counterparts. Vacuum-deposited and/or sputtered resistor networks of sufficient accuracy for use in 7- to 10-bit converters are being developed.

Masks employed in photoresistive operations, whether laid out by hand or machine, are marginal in accuracy with respect to the present application. The nature of the difficulty may be understood by considering the tolerance on width of a resistor line in a 10-bit (0.1 percent) decoder. The nominal width is two mils. The permitted error in width is two microinches: it is known that averaging of errors acts to reduce the tolerance requirement on individual portions of a resistor. Layout techniques designed to maximize this averaging are being studied. Sheet resistance of deposited material must be tightly controlled but probably

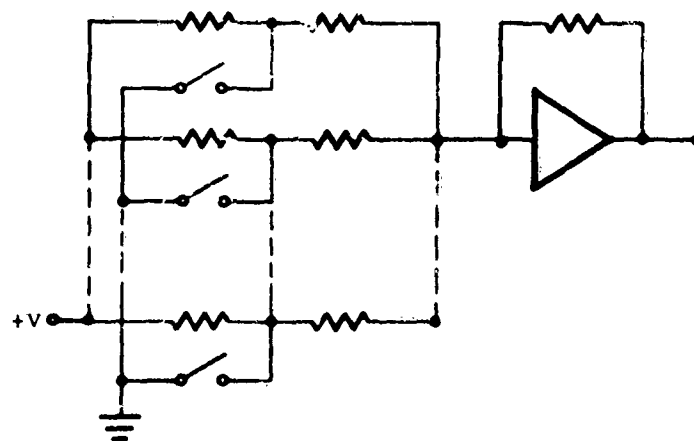


FIG. 11a WEIGHTED RESISTOR DECODER

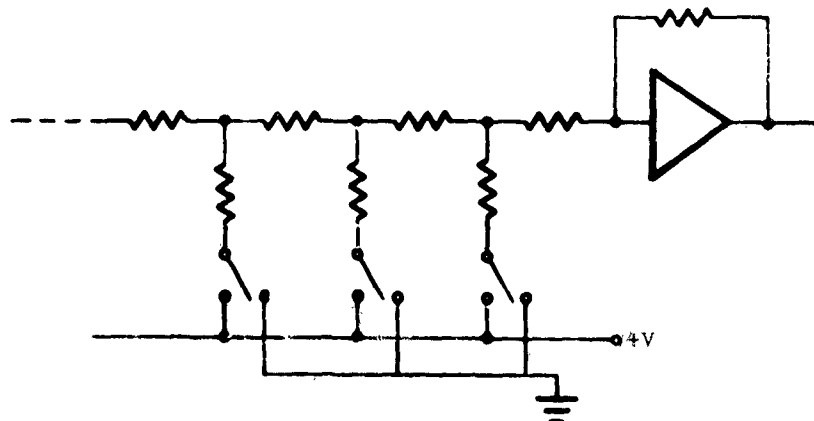


FIG. 11b LADDER DECODER

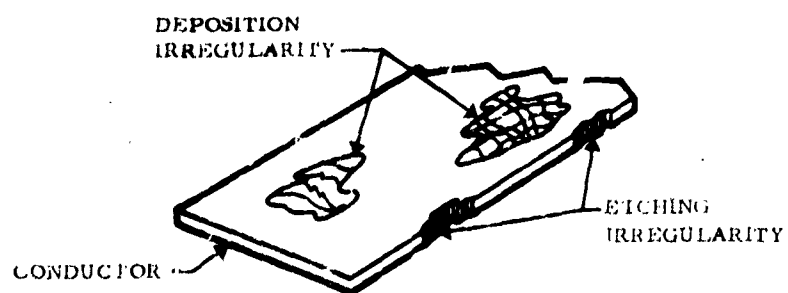


FIG. 11c THIN FILM IRREGULARITIES

Figure 2-78. Weighted Resistor Decoder, Ladder Decoder and Thin-Film Irregularities

can be achieved by extension of existing techniques. Etching processes for this application will require additional closed-loop control techniques not yet extant. Electron microscopic studies may be used to reveal etching and deposition induced irregularities that must be controlled.

Optical Types

Under contract NOW 65-0467-c, issued by the Bureau of Naval Weapons, Litton will develop a single turn 2^{15} GaAs optical encoder, with a size 18 standard servo mounting. This device will incorporate all integrated circuitry in its output electronics and will meet severe shock and vibration requirements.

Nuclear Radiation Types

Under contract NOW 65-0467-c from the Bureau of Naval Weapons, feasibility studies will be performed by Litton leading toward the development of encoders using nuclear isotopes as radiation sources. Feasibility of such a technique was indicated by developments at Litton in 1964, which preceded award of the referenced contract. The specific devices to be developed under the contract will be single turn size 18 encoders yielding a natural binary output of 2^{13} to 2^{15} . The radiation source will be Americium, which has a half life of 470 years. No external power is required for such a means of interrogating the code disc and only minimal power is necessary to operate the electronic output circuitry. It is anticipated that nuclear encoders will find applications where resolution and accuracy required is moderate and very low power is available.

Hall Generator Devices

Frequently Hall effect devices are suggested for use in D-A conversion and in multiplication circuits. The extreme simplicity of the basic effect has lead many investigators to pursue these approaches. In connection with such programs as that which lead to the selection of our hybrid computer building blocks we have reviewed the situation and can submit certain observations.

Zero point errors associated with the cancellation of longitudinal voltage drops militate against low level applications. Linearity is good in respect to the current required to produce the magnetic field. The difficulties of designing a magnetic circuit (with air gap to accommodate the Hall material) that is at once both small and linear are formidable. The

best techniques are those which involve a second sensor of the magnetic field in a feedback circuit. Even that approach is limited by the non-homogeneity of the magnetic field in a structure of small dimensions.

Notwithstanding the extensive governmental support of Hall devices in connection with twenty or more independent programs ranging from aerospace to animal husbandry, techniques have not been developed which permit Hall devices to be readily produced with accuracies must better than one percent.

2.4.5 Summary and Conclusions

Future generation weapon systems demonstrate the following trends in conversion systems:

1. A tendency to digital computation in the entire avionics.
2. All electronic conversion techniques.
3. Distributed conversion systems.

These trends are made possible primarily by advancements in monolithic silicon and thin film technology. The result will be a more reliable interface between the computer complex and the equipment it services. This will also be accompanied by a weight reduction as the need for electromechanical conversion decreases.

III DISPLAYS/CONTROLS

3.1 GENERAL

Electronic displays included in avionics systems now under development constitute the primary communication link to the air crew for the following categories of information:

Current status

Commands for immediate action

Prediction information for future action

Within these categories can be encompassed virtually every essential mission task. The necessary data and information to be presented on the displays is obtained from a wide variety of sources, including the central processing system, the potentially many sensors, photographic slides, and sometimes directly from communication channels.

In accordance with current human engineering precepts, the situation displays are segmented into three types: 1) the head-up display; 2) the vertical situation display; and 3) the horizontal situation display. System requirements imposed on these displays include brightness/contrast, resolution, accuracy, format flexibility, field of view, data rate, storage time, stabilization, MTBF, etc. Physical requirements imposed include total volume, form factor, weight, cooling, ruggedness and power. These requirements, in total, comprise a continuing challenge to the display art. In the effort to meet these requirements, improvements to existing technology as well as new solutions are continuously being sought.

The existing technology is predominantly CRT in black and white, both of the conventional indicator type as well as the direct view storage tube. These types, in their many varieties are reviewed herein. New

aspects of this technology, at least insofar as avionics is concerned, are the use of scan conversion and color tubes. Both these aspects show much promise for future systems. A radically new approach would eliminate the CRT and substitute an electroluminescent panel. The EL panel could portray situation information as well as typical status information as displayed on dials, tapes, etc. The potential for EL is assayed in light of current experimental and development work in progress.

Two other topics, while not of such major significance as the above, are included in this review. The first of these is concerned with the comparative evaluation of analog vs. digital techniques in such areas as sweep and symbol generation. Secondly, brief consideration is given to displays of the fixed format type which are often used for conveying status and control information.

3.2 CATHODE RAY TUBES

Historically, the cathode ray tube has found its greatest application in the display of information derived from radar equipment; in recent years this use has been expanded to include the display of computer-processed information. As a result, most of the CRTs available are quite conventional, differing only in size or shape of envelope, or type of electron gun. However, due to the rapidity of action and great versatility of the cathode ray tube, it was also applied to other applications, including recording, electronic image generation, production of color, and projection. These applications have led to the development of special tubes, with the particular characteristics required for the application.

3.2.1 General-Purpose Types

General-purpose cathode ray tubes break down into two major types; electrostatic or electromagnetic, defining the type of deflection used. The type of focus is also used to additionally define the electromagnetic type, since either electrostatic or electromagnetic focus is utilized. Different types of guns are utilized for different applications of both types of CRTs; in general, however, the gun type selected only affects the biasing requirements.

NOTE

In specifications, EM is used to characterize electromagnetic, and ES to characterize electrostatic. Thus, EM-ES refers to an electromagnetic deflection type with electrostatic focus.

The choice between the electrostatic deflection type and electromagnetic type of cathode ray tube is dependent upon the amount of material to be displayed and the desired size of the display. The electrostatic tube is a voltage-operated device, and the electromagnetic tube is current-operated. Thus, where high speed deflection is required, the usual choice is the electrostatic type. However, for large tubes, the deflection voltages for the electrostatic type become very high, with a requirement for dynamic focus and astigmatism correction; then the electromagnetic type is to be preferred. The electromagnetic tube offers advantages in having better focus characteristics; also, because of its requirement for high current-low voltage driving circuitry, it is more easily completely transistorized. Because of an inherently simpler gun structure, the coupling to the grid is much easier; the electrostatic tube control grid is usually biased at a high voltage, while the electromagnetic tube grid is operated around ground. Additionally, the yoke driving circuitry is completely isolated from the gun, while with the electrostatic tube the deflection amplifiers are usually biased at a high voltage. Thus, both types of tubes have advantages, and the choice is strictly dependent upon the particular requirements of the display.

Tables III-1 and III-2 indicate typical types and sizes of general-purpose cathode ray tubes. A simple comparison between the electrostatic and electromagnetic types of the same faceplate size will quickly indicate the difference in length between the types.

3.2.2 Dual Deflection Type

A modification to the basic electromagnetic type of CRT has been the addition of deflection plates to the gun; these plates are capable of a limited area of scan, but can be used for describing symbology. In this fashion, the advantages of the electromagnetic tube can be utilized and the symbols can be painted at the high rates possible with electrostatic deflection. Figure 3-1 is an illustration of this type of tube. Characteristically, the deflection factor for the deflection plates is 185 volts/inch. Tubes of this design are manufactured by Raytheon (as CK 1357),

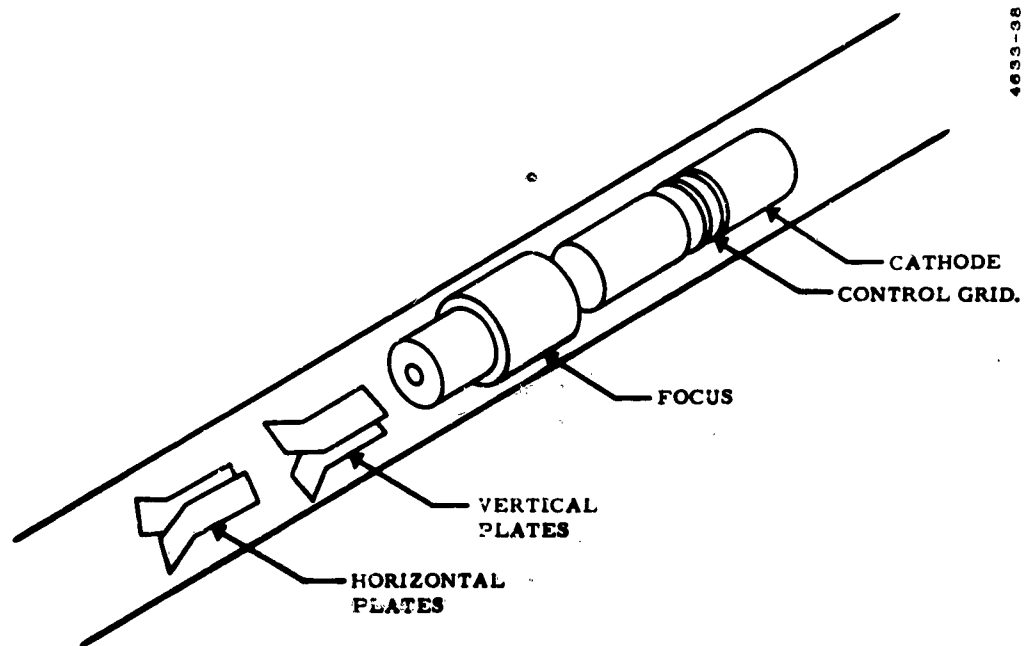


Figure 3-1. Gun Structure, Dual Deflection CRT

TABLE III-1
ELECTROSTATIC DEFLECTION - ELECTROSTATIC FOCUS

Dumont Outside Face Overall Curvature Accelerator 10,000 3500 to 4100 145 to 215 100 to 160 110 to 170 0.012 #2

Dumont Outside Face Overall Curvature Accelerator 10,000 3500 to 4100 145 to 215 100 to 160 110 to 170 0.012 #2

Type	Outside Face Dimensions (inches)	Overall Length	Faceplate Curvature	Post Accelerator	Accelerator	Focus	Grid Cutoff	Deflection Factor (V/inch)		Line Width
								D1-D2	D3-D4	
3BEP	3	13 3/4	Flat	1500	500	25 to 125	30 to 60	12 to 15	9 to 12	0.030
5AMP	5 1/4	17 5/8	Flat	-	2500	0 to 300	34 to 56	40 to 50	20 to 25	0.30
7AEP	7	15 1/2	Flat	4000	2000	380 to 620	45 to 75	81 to 101	67 to 83	0.22
10ALP	10 1/2	20	12	-	8000	2250 to 3100	105 to 205	155 to 189	141 to 185	0.012 @ 200 μa
12AMP	12 7/16	23 1/8	10	9200	5300	1450 to 1750	11.5	105 to 117	105 to 117	0.020 @ 200 μa
15AMP	16 1/8	27 3/4	27	12,000	7500	1760 to 2670	160 to 240	96 to 150	96 to 150	0.020
Dumont KC2395	19	31 7/8	53	18,000	10,000	3500 to 4100	145 to 215	100 to 160	110 to 170	0.013

TABLE III-2
MAGNETIC DEFLECTION

R-6238P Dimensions 22 1/16 56 5/16 Angle Faceplate Deflection Accelerator Grid -45 to -70 ES 1400 to 0.0065 200

Type	Face Dimensions (inches)	Length	Faceplate Radius	Deflection Angle	Accelerator	Grid #2	Grid Cutoff	Focus	Line Width
3AKP	3	6 3/8	Flat	35°	7000	300	45 to 95	ES -105 to +250	0.011 @ 50 μa
5AHP	4 15/16	11 1/8	24	53°	5000	300	28 to 42	ES-0 to 200	0.010 @ 100 μa
5DKP	4 15/16	11 1/8	24	53°	8000	250	36 to 70	EM	0.0565 @ 200 μa
7MP	7 3/16	12 3/4	24	50°	7000	250	25 to 70	EM	0.011 @ 200 μa
10SP	10 1/2	16 5/8	42	50°	12,000	200	18 to 48	ES 1400 to 1900	0.017 @ 100
10AKP	10 1/2	17 3/4	42	50°	9000	650	40 to 70	EM	0.012
12ABP	12 7/16	18	40	55°	10,000	300	28 to 72	ES0 to 300	0.017 @ 100
12SP	12 7/16	18 3/4	40	54°	9000	250	27 to 63	EM	0.015
16AKP	15 7/8	22 1/16	56 5/16	53°	12,000	300	35 to 75	ES -300 to +250	0.030 @ 100 μa
16ADP	15 7/8	21 5/8	40	53°	12,000	250	27 to 63	EM	0.020
17QCP	12 1/4 X 15 3/8	19 1/4	27	70°	5000	300	28 to 72	EN	0.025 @ 100 μa
Dumont K2267	18 5/8	22 9/16	28	66°	10,000	500	51 to 99	ES 190 to 300	0.018 @ 25 μa
22CP	21 3/4	22 1/16	165	70°	15,000	300	33 to 77	EM	0.050
Rauland R-6238P	24 1/32	25 1/16	180	70°	18,000	400	-45 to -70	ES -300 to 0	0.25

Dumont (as 19WP-), and Sylvania (as SC-3185), as well as Litton Tube Division and Thomas. Sylvania also produces a tube of this type, with rear optical port, and is described in the section on optically-ported tubes.

Although this type of tube does offer the advantages of high-speed character writing, care must be taken in its use; shadowing of the beam pattern by deflection of the beam within the plate area or distortion of the pattern by fringe magnetic fields of the yoke are typical of problems that can be encountered. These problems can be avoided by careful selection of the tube (location and size of the plates relative to the center of magnetic deflection), the yoke (length), and by use of shields to restrict the magnetic field.

3.2.3 Special Purpose Cathode Ray Tubes

For the many special applications of cathode ray tubes, specialized tubes have been developed, either to permit CRTs to be utilized more efficiently, to improve on their characteristics, or to offer new uses. This section will describe these specialized cathode ray tubes.

3.2.4 Multi-Gun Cathode Ray Tubes

With an ever increasing amount of data to be displayed, the logical step has been to increase the number of electron guns in the CRT; this is necessary when either the amount of data to be displayed exceeds the capability of one gun, or when the time sharing of the one gun cannot be allowed due to the loss of primary data. Typical of this is the display of radar derived video, with interruption for symbology.

Electrostatic multi-gun CRTs have been produced in various sizes, with up to ten guns used. However, most of the designs using more than two guns have been developed for applications where registration of the beam is not a requirement. Typical multi-gun electrostatic CRTs are tabulated in Table III-3.

Although it sounds quite impractical, dual gun electromagnetic cathode ray tubes have been developed. In one type, the Rauland R-6239, illustrated in Figure 3-2a, two necks are used. In a second type, a Raytheon development, one on-line gun and a second offset gun are used. This second type is illustrated in Figure 3-2b.

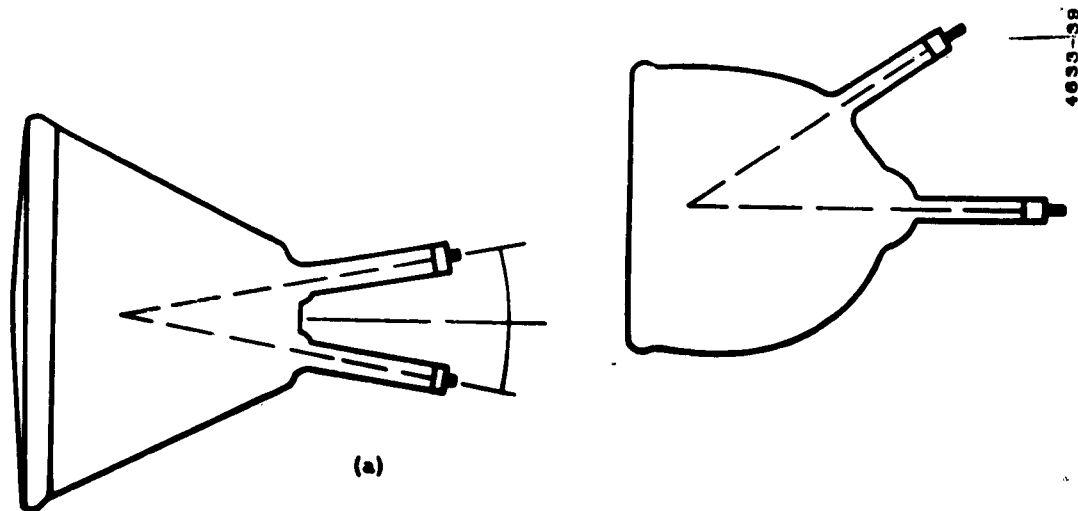


Figure 3-2. Electro-Magnetic Deflection CRTs

TABLE III-3
ELECTROSTATIC MULTI-GUN CATHODE RAY TUBES

Type	Face Plate Size	Guns
Sylvania SC3090	5 1/5 X 5 1/2	3
7DP7	5 1/2 X 5 1/2	5
Dumont K1098	5 1/4"	4
Sylvania SC3561	6 1/32 X 4 1/32	3
Sylvania SC3061	10"	3
Sylvania SC3399	10"	5
12ACP	12"	2
Sylvania SC 4096	12"	2
Sylvania SC 4327	16"	
Dumont K2303	20 1/4"	2

Although inherent interaction (crosstalk) between the deflection yokes will result in deflection errors, and offset guns require "keystone" corrections, by proper shielding of the yokes and guns, and electronic compensation, these deteriorative effects should be eliminated.

3.2.5 Optically Ported Cathode Ray Tubes

In some applications it is necessary to continuously display a fixed format, such as geographic map, on the CRT screen while changing other data. By placing an optical port in the rear of the tube, the fixed data may be projected onto the CRT screen from slides in a projector, while computer-derived or real-time (such as radar) data is displayed using the electron beam. The slides may be changed to permit range scaling of offsetting of the display.

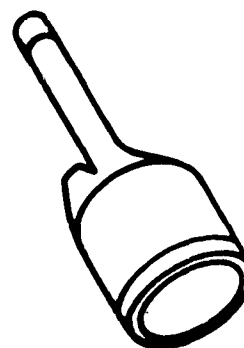
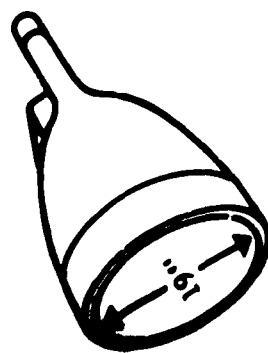
Figure 3-3 illustrates two optically ported cathode ray tubes, one a 19" and the other a 7" tube. Both of these tubes have one port; other tubes have been produced with up to three optical ports. The ports, besides being used for projection of fixed data, can be used for filming the display, where a permanent record of the displayed data is desired.

While virtually all of the available optically ported CRTs are magnetic deflection, there is no reason any type of gun cannot be put into an optically ported envelope. Optically ported tubes have been fabricated using beam shaping guns; the illustrated 19" tube utilizes the dual deflection gun described earlier, and was designed as a replacement for another CRT where the required map display was accomplished using scanning and video from a flying spot scanner.

In the use of an optically ported CRT, the optical corrections necessary to avoid distortion in the projected picture and the screen characteristics of the phosphor cannot be neglected. Ideally, the projected picture should differ from the electronically painted picture in color, so as to avoid confusion of the two sets of information. This requires careful selection of the phosphor and projected colors.

3.2.6 Beam-Shaping Cathode Ray Tubes

As was noted earlier, one method for the generation of a symbol on the CRT screen is by moving the electron beam so as to describe the desired figure. A second way is to form the electron beam so as to



4693-40

Figure 3-3. Optically-Ported CRTs

form the figure, much as in an extrusion process. Several cathode ray tubes have been developed using this technique; one type, the Charactron, is illustrated in Figure 3-4. In the tube, a stencil-like matrix, a thin disc with alphanumeric and symbolic characters etched through it, is placed in front of the electron gun. A stream of electrons emitted from the gun is extruded through the selected character of the matrix. Thus the beam is formed, and when it hits the phosphor screen the character is reproduced. A large aperture is provided in the matrix for those operations where a focused spot is desired.

After the beam has passed through the matrix and has been shaped, it is directed back on axis by the convergence coil and reference plates, with a deflection coil used to position the beam on the appropriate spot of the screen.

Normally, 64 characters are etched into the matrix, but, where required, as many as 200 can be fitted into the matrix. Variable character size can also be obtained. Larger characters require a longer paint time, of course, to obtain the same brightness.

With the number of elements in the gun structure, this type of tube is necessarily long; a 19" tube is 34" long, as compared with the 31-7/8" for an equivalent electrostatic type, 22-9/16" for an electromagnetic type, and 24-11/16" for a dual-deflection type. Where this length cannot be permitted, a more compact electron gun is used, referred to as the APSEL (for aperture selection) type. In this type tube, the entire character matrix is flooded with electrons; the following selection plates direct the beam against a selection screen containing an aperture so that only one character may pass through. In this fashion, the desired character is selected, and the convergence coil and reference plates are eliminated. The energy of the selected character beam is quite low, and more time is required for character writing than with the conventional Charactron. The APSEL gun is illustrated in Figure 3-4.

By combining the aperture selection technique with a fiber optics faceplate, a CRT for use in high speed printing has been developed. This is the Charactron G3061, shown in Figure 3-5. The operation of the gun is exactly as described for the conventional Charactron, but the faceplate is comprised of an 8.5" X 0.5" fiber optics strip. The deflection of the formed beam is only in the horizontal axis, along the fiber optic strip, for page-width printing. See Figure 3-6.

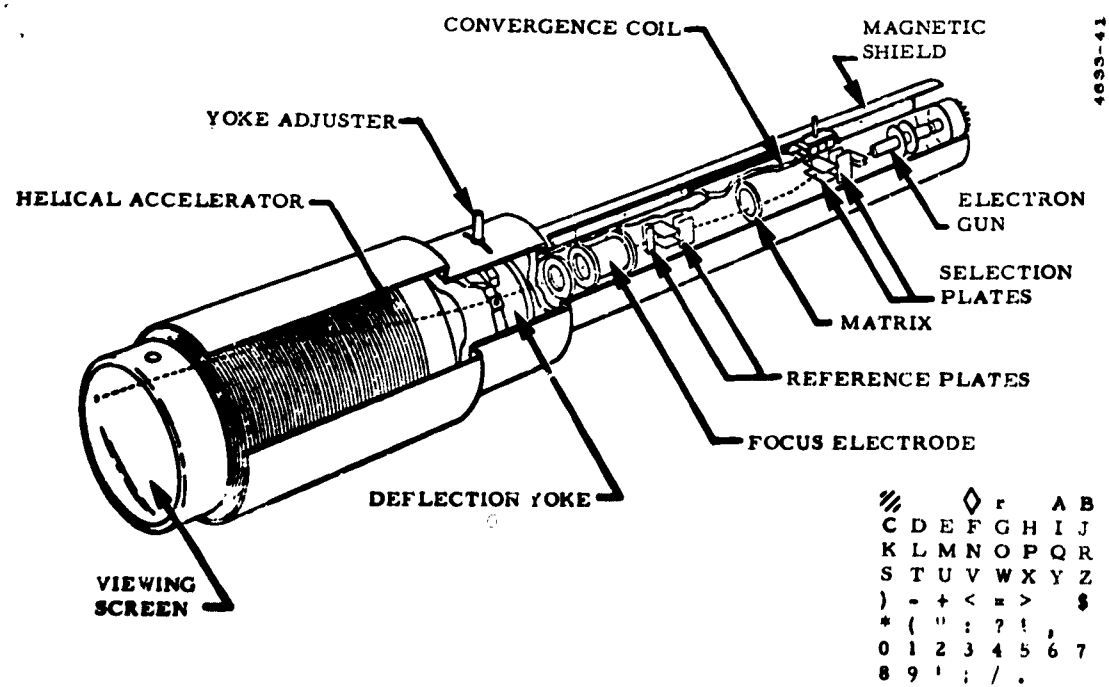


Figure 3-4. Charactron Display CRT (With typical matrix)

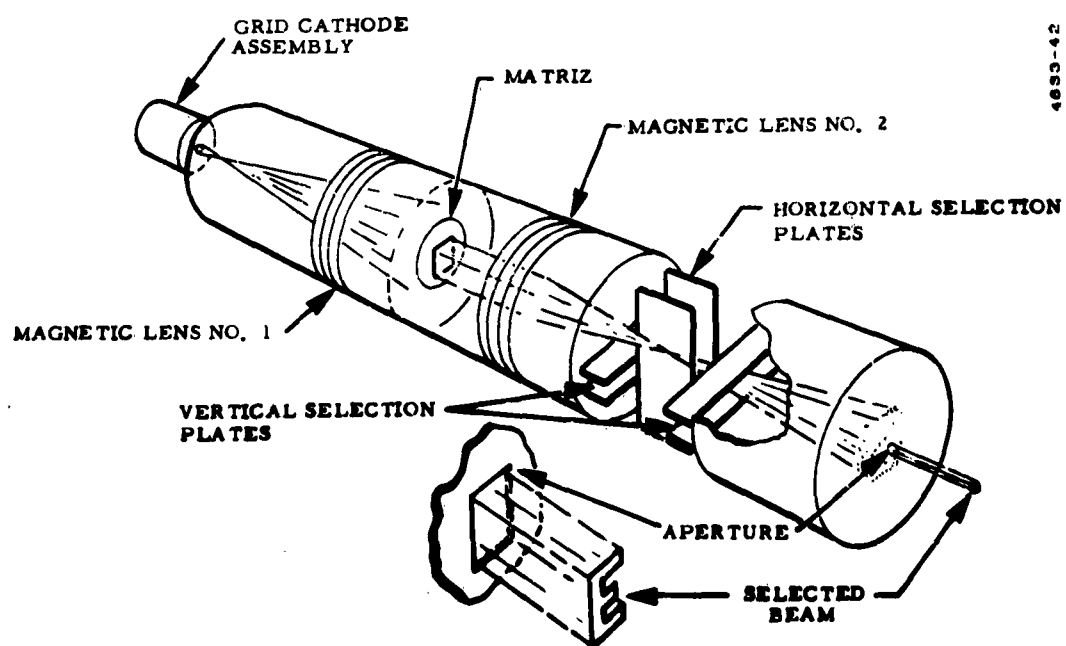
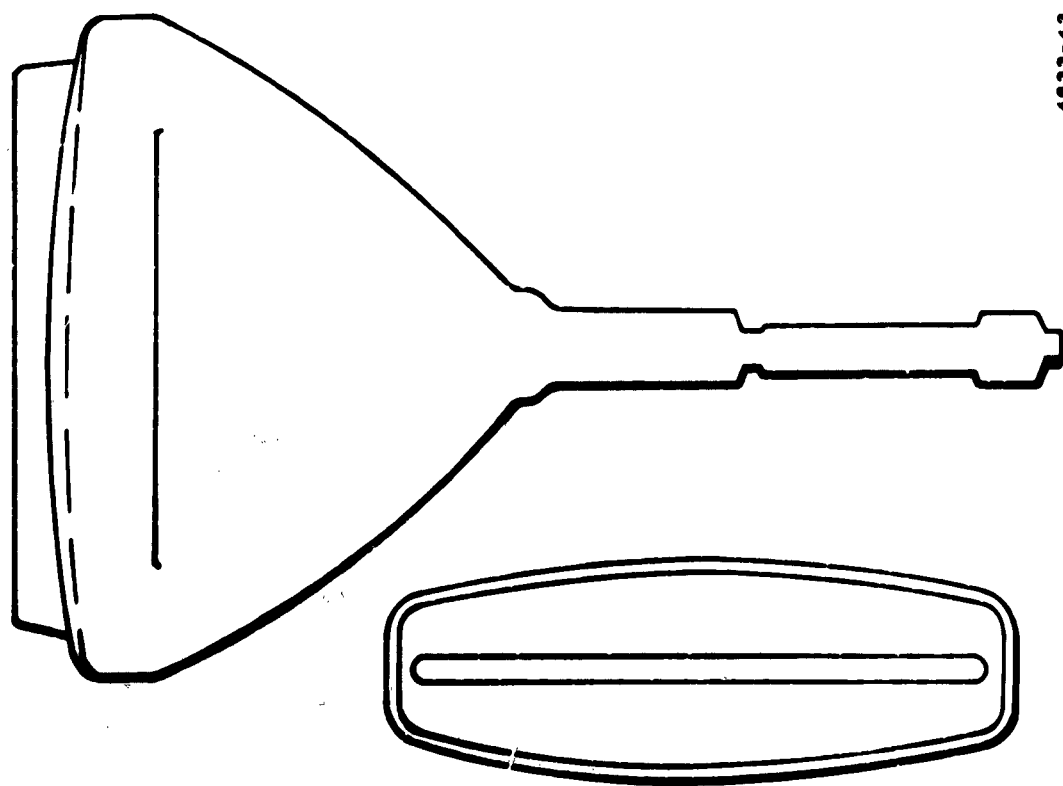


Figure 3-5. Aperture Selection Beam-Forming Tube



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Figure 3-6. Charactron With Fiber-Optics Faceplate

Another variation of the beam shaping tube utilizes a storage tube construction, with the write gun being the beam forming type. This is the Typotron tube, illustrated in Figure 3-7. The electron gun operation is basically as described for the Charactron; the screen construction is that of a conventional direct view storage tube, with storage mesh, collector mesh, and flood gun. This tube type has been widely used in Air-Traffic-Control display consoles, with good results.

3.2.7 Character Generation Cathode Ray Tubes

Beam forming cathode ray tubes, the Charactron and Typotron, as described in the previous section, generate characters directly in the tube, and no external symbol generator is required. Another class of specialized cathode ray tubes generate symbols for use in other displays, effectively replacing the conventional electronic symbol generators. These tubes are referred to as Character Generation Cathode Ray Tubes.

One type of character generation CRT, the Monoscope, built by several companies, has been used widely; in conjunction with an electrostatic discharge (wire grid faceplate) tube, it is used for forming and printing address labels for machines.

The operation of the monoscope tube, illustrated in Figure 3-8 is dependent upon the effect of secondary emission. The target is an aluminum character, on a carbon-ink background. As the target character is scanned by the electron beam, the secondary emission from the target is collected by the collector, resulting in a video signal. This signal, transmitted to other CRTs where their phosphor screen is scanned in synchronization with the plates of the monoscope, results in the formation of the scanned character. Although the target shown in the illustration is that of a single character, the target can be comprised of up to 64 characters; to form a selected character, the beam is deflected to the desired character and the character is then scanned, to form the video for that character.

Another type of character generation CRT is the Matricon, illustrated in Figure 3-9. The target is comprised of conducting elements, isolated from each and mounted on an insulator. The electron beam is scanned over the target matrix, in raster form, with the display CRT utilizing the formed character also being scanned, in synchronism. By selection

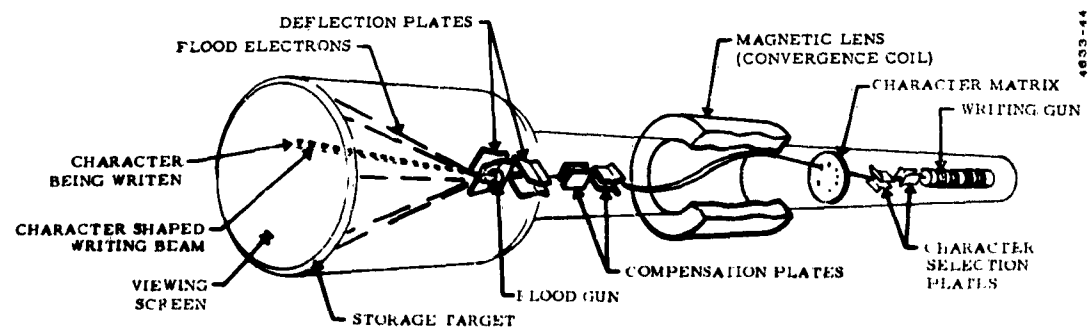


Figure 3-7. Character-Forming Storage Tube (Typotron)

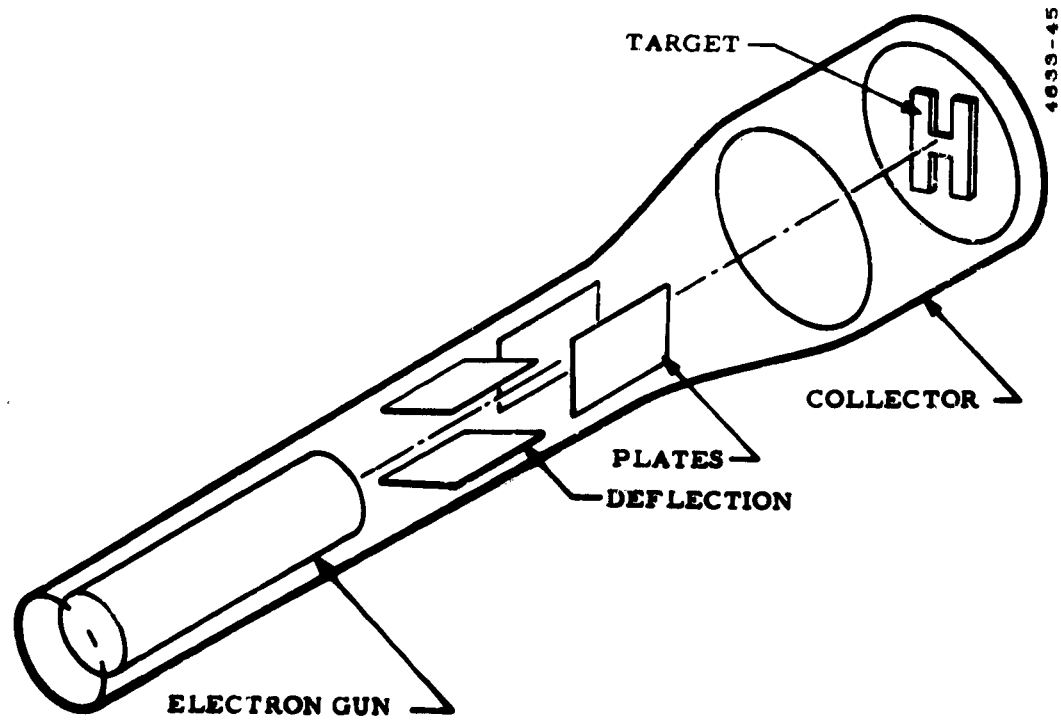


Figure 3-8. Monoscope CRT

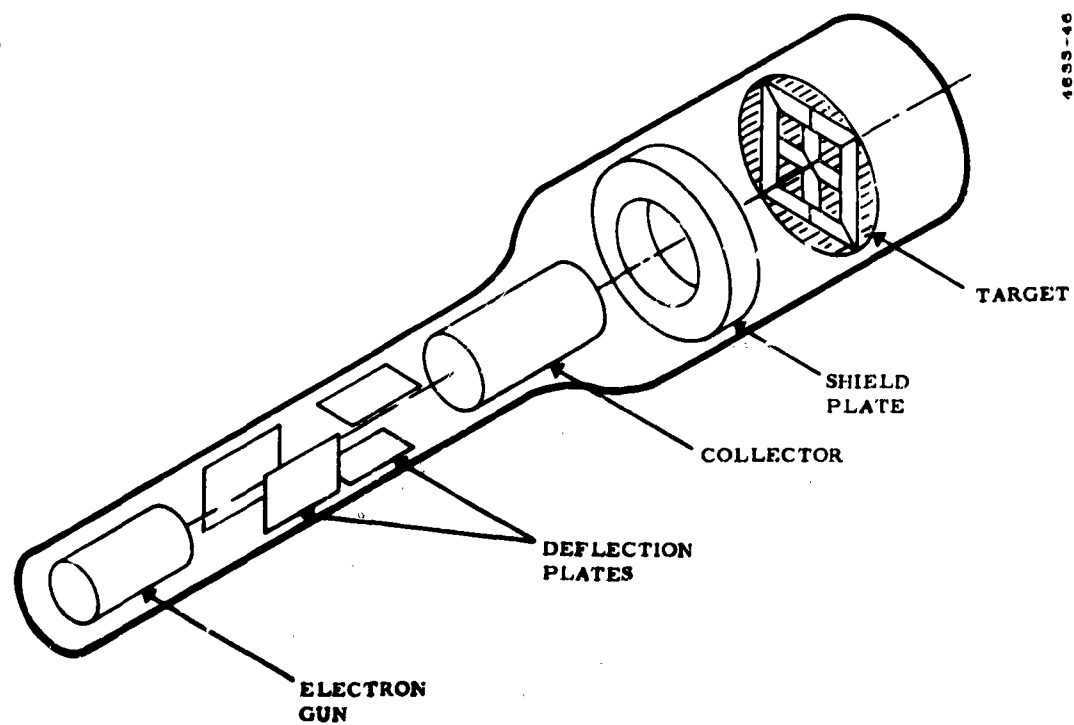


Figure 3-9. Matricon

of the matrix elements, either the electron beam is permitted to hit the element or it is repulsed, and collected at the collector. Thus, by selection of the proper elements, a video signal is formed at the collector that accurately describes the character. A decelerator mesh and shield plate are used to control the electron optics of the tube.

Figure 3-10 depicts a typical seven element matrix for the Matricon, and a typical numeric formed with this matrix.

If the matrix elements of the Matricon were not switched, and the signal from an impinging electron beam were sensed at each element, a CRT switch could be formed. This is similar in operation to the cathode ray switch tube, described in the section on "one-of-a-kind" tubes.

3.2.8 Projection Cathode Ray Tubes

Specialized cathode ray tubes have been developed for projection displays; these differ from conventional CRTs because of the very high light output required. To achieve the high light levels, the tube is generally operated at very high voltages (as high as 80 KV), with the screen and face design optimized. This includes faceplate curvature to match the optical system, polished optically to eliminate small flaws, and a thick aluminized screen.

Projection CRTs of the electromagnetic type are made in sizes up to 7". Typical light output of a 5" projection CRT operated at 27,000 volts, is 4000 foot-lamberts. Operating at these levels, forced air cooling is required to prevent damage to the screen. The glass used in the faceplate must be a special non-browning type, since under bombardment glass tends to discolor and thus reduce the transmitted light.

Numerous difficulties have prevented the widespread use of projection CRT systems other than for theater TV. These include the short life of the CRT and the problems associated with x-ray shielding and the extremely high voltages used. And, even with the best optical systems, the light level at the screen is barely acceptable, even for a darkened theater. The Raytheon Components Group is presently engaged in the development of a projection CRT, where the faceplate is metal, in contact with and cooled by water, and the phosphor screen is deposited directly to the metal. Projection is thus through the back of the tube, from the same side as the impinging electron beam; brightness achievable is stated at 25,000 foot-lamberts with a 3 X 4 raster.

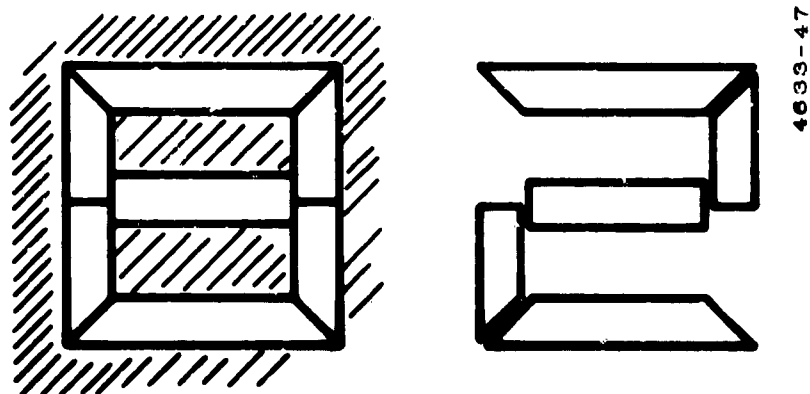


Figure 3-10. Seven-Element Matricon Target and the Numeric Formed by Selection of Elements

Another form of projection CRT utilizes a special screen of potassium chloride (KCl), which darkens under electron bombardment. Light is then either reflected off the screen or is projected through it, to form the image. This KCl screen has low contrast and excessive persistence, however, and its application has not been extensive.

With the development of the direct-view storage tube, with its exceptionally high light output at low voltage levels, this type of tube has also been adapted to projection displays. Tubes of this type are described in the section on direct view storage tubes.

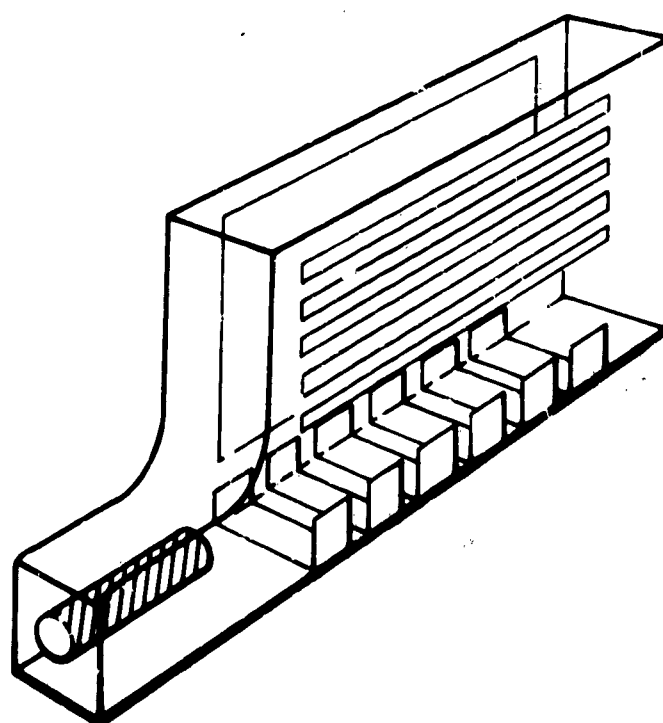
With the development of the light valve projector, and the improvement of film projection systems, the CRT projection technique has been supplanted, and will continue so until new tubes are developed.

3.2.9 The Kaiser-Aiken "Thin" Cathode Ray Tube

One of the most often voiced complaint against the use of cathode ray tubes has been the large volume required, when such a small portion of the tube is actively used. With the utilization of microcircuits in displays, the large volume required becomes even more apparent. The importance of reducing the tube dimensions is most evident in aircraft and tactical display systems.

The Kaiser-Aiken Thin CRT is notable in the reduction of the CRT volume. The principle of its operation is illustrated in Figure 3-11. The tube envelope is constructed of two glass sides, held apart by glass spacing edges that complete the vacuum seal. Along the inside of one side the phosphor screen is deposited; along the inside of the other side, transparent conducting strips are deposited, to serve as vertical deflection plates. Along the bottom edge of the tube, metal channel elements, isolated from each other, are mounted to serve as horizontal deflection plates.

The electron beam is injected along the bottom of the tube, passing through the U-form of the horizontal deflection plates. When the voltage on a deflection plate is lowered, the beam is deflected upward. The point at which this occurs thus can be controlled by selecting which electrode voltage is lowered.



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Figure 3-11. Kaiser-Aiken "Thin" CRT

The same action results with the vertical deflection plates, and the beam is directed toward the desired point on the phosphor screen. For linear, well defined pictures, at least two adjacent deflection plates must be operated in an overlap fashion, so as to both contribute to the deflection of the beam.

The thin cathode ray tube has several advantages, other than its thin construction. The deflection-focusing action results in an improved spot size, rather than a defocusing action; the tube, utilizing transparent tin oxide for the vertical plates and transparent phosphors, can be made completely transparent for see-through operation (such as cockpit "heads-up" displays). One of the drawbacks, up to now, has been the mechanization of the deflection circuitry. Besides having to operate at elevated voltage levels, the selection of the particular plate (or plates) for display has presented difficulties that have prevented its use in jump-scan modes, although several techniques have been developed for generation of raster scan deflection.

The capability of the thin CRT for presentation of color (discussed in the section on color CRTs) has resulted in a continued interest in the technique, even where the volume saving is not of great importance.

3.2.10 Cathode Ray Tubes for Recording and Printing

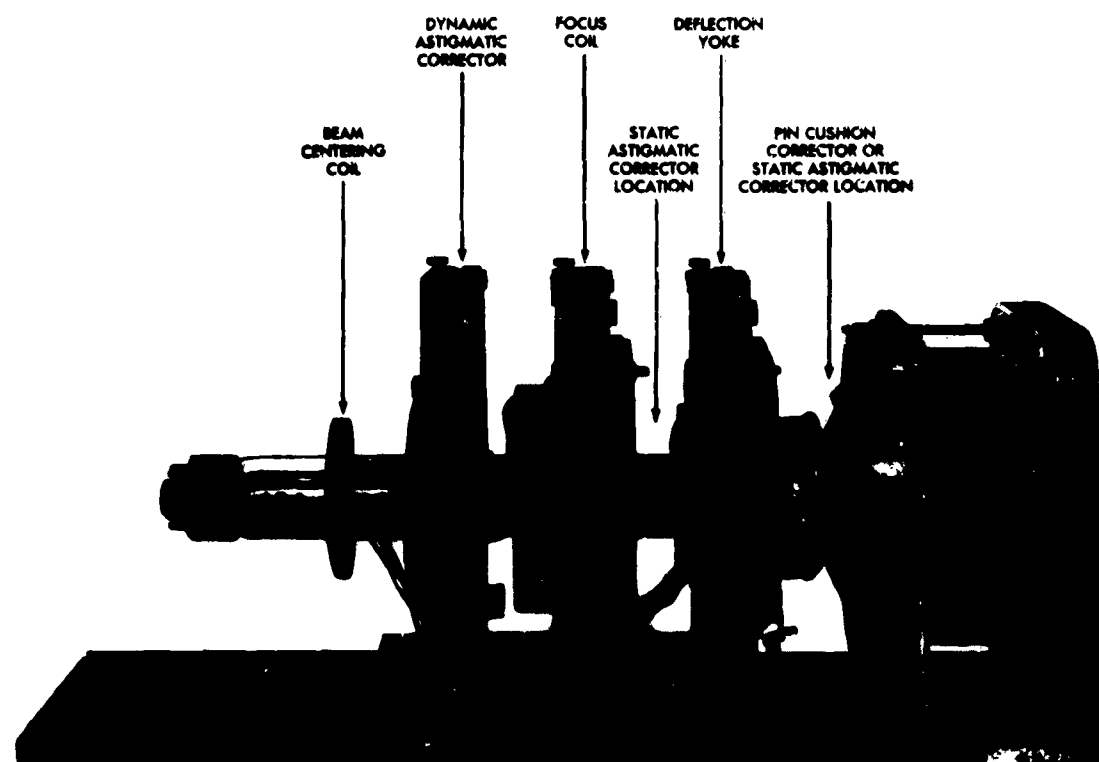
Due to the speed and flexibility of cathode ray tubes, their application to recording and printing has been a logical step. The simplest form of CRT-Recorder is the oscilloscope-camera combination, commonly used for laboratory waveform recording. Cathode ray tube photographic film recorders are also extensively used for recording of computer-formatted and radar displays for storage and large screen displays. In most cases, conventional cathode ray tubes are used for these applications; due to the requirement for small spot size, magnetic deflection-magnetic focus type are usually used.

The need for high-speed recording equipment has brought about development of new recording materials and techniques. One characteristic of most of the new materials (Kalvar, Photochromic) is their low sensitivity. This has in turn brought about the development of special cathode ray tubes, capable of developing the required energy output for use with low sensitivity materials. The approaches taken have been to reduce the spot size of the CRT (improved gun design), to make more efficient use of the emitted energy (fiber-optics faceplates), and high energy output (while still avoiding damage to the phosphor screen). Cathode ray tubes typical of these techniques will be discussed in this section.

3.2.11 High Resolution Cathode Ray Tubes

To take advantage of the very high resolution capabilities of the recording materials available, cathode ray tubes have been developed with spot sizes of 0.001 inch and less. Typically, these tubes are electromagnetic deflection, electromagnetic focus, although some types have achieved these very low spot sizes with electrostatic focus. Extreme care is required in the construction of these tubes. They are built with exceptionally uniform, fine grain, low noise, phosphor screens deposited on an optical quality faceplate.

To achieve the specified spot sizes of these high resolution tubes, it is necessary that the associated coils be accurately positioned, and that the power supplies for the tube and the coils be tightly regulated. The coils are generally mounted rigidly in an assembly that also holds the CRT, with the mounts designed to permit precision adjustment of the coils in several axes. Figure 3-12 is a typical such "Micropositioner" assembly.



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Figure 3-12. Micropositioner Assembly with High Resolution CRT

With the development of the newer (but low sensitivity) recording materials, it was necessary to increase the light output of the recording CRTs, to achieve exposure in a reasonable length of time. The increase of power inevitably results in spot size growth, and thus a loss of resolution. The development of fiber optics faceplates, with its better light utilization, together with improved electron guns, has now made it possible to expose the newer materials directly from a CRT.

Fiber optics used in faceplates offer tremendous advantages over conventional cathode ray tubes. No scattering of the light is experienced as it is transmitted through the faceplate, unlike that experienced with a conventional glass faceplate. The recording material can be placed directly against the face, thereby avoiding the light loss experienced in lens transmission. A CRT equipped with a fiber-optics faceplate is shown in Figure 3-13.

3.2.12 Line Scan Tube

A serious drawback to the use of cathode ray tubes in line scan recording applications (where the recording line is stationary and the recording medium is fed past the recording unit) has been the limited radiant energy output of the phosphor without damaging the screen. In a conventional CRT, the phosphor is deposited on glass (having low thermal conductivity), and high beam current results in high local temperatures and the resultant damage. Where the beam is scanned in both a vertical and horizontal directions, high peak currents can be used without exceeding the permissible point power level.

The CBS Line-Scan Tube, illustrated in Figure 3-14, effectively accomplished this through the use of a rotating, phosphor coated anode. Since successive lines are not painted in the same place on the phosphor, high beam currents can be utilized and high light output obtained.

This construction technique offers several advantages over the use of a conventional CRT for line scanning, besides avoiding damage to the phosphor at high beam currents. Since the phosphor is viewed from the same side as it is energized by the electron beam, the scattering of the light and the transmission loss of the phosphor is eliminated. Secondly, the "streaking" in the recording from a conventional tube due to defects in the screen is avoided, since the phosphor area being scanned is continually being changed.

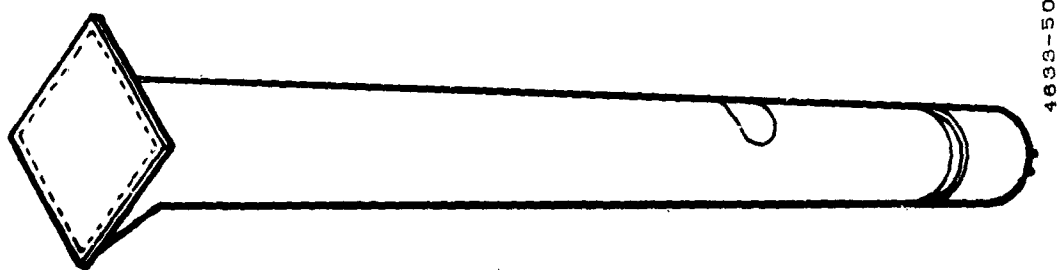


Figure 3-13. Cathode Ray Tube with Fiber-Optics Faceplate

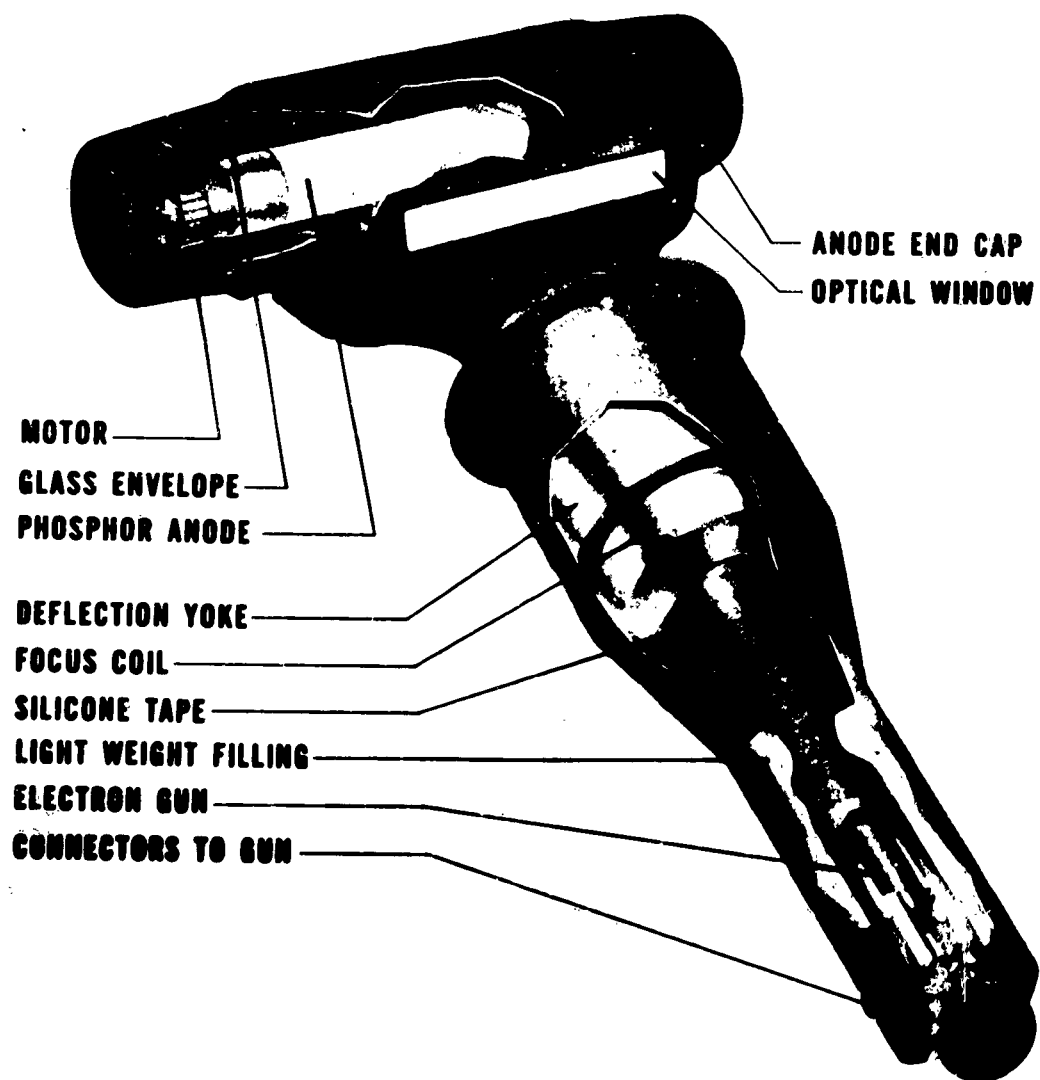


Figure 3-14. CBS Line-Scan Tube

A graph of contrast vs. resolution for a typical line-scan tube is shown in Figure 3-15. This curve was obtained by scanning a bar chart transparency with an optical image of the light spot from the LST.

3.2.13 Electrostatic Discharge Cathode Ray Tube

The same characteristics of high speed and flexibility that make the cathode ray tube attractive for recording apply to high speed printing equipment. The Electrostatic Discharge Cathode Ray Tube has been developed for utilization in printing systems employing the principle of electrostatic charge deposition.

In electrostatic charge deposition printing, a charge pattern is laid down in the forms of characters, symbols, or picture elements, and the dielectric is then lightly dusted with an electroscopic powder. For a permanent record, the printed material can be set. Several processes have been developed for depositing the charge patterns, including Xerography and Electifax. Another process involves the use of a switchable matrix of fine wires, in contact with dielectric, and brought up to voltage by means of electronic switches.

The Electrostatic Discharge CRT utilizes this last principle; the wire matrix is made the faceplate of a CRT, and the wires are charged through the use of the electron beam. A tube of this type is illustrated in Figure 3-16.

CRTs of this type have been produced by both Sylvania and Litton Tube Division. Sylvania has developed one type, the SC-2795, where the matrix of wires is 0.16 x 2.75 inches, and can be used to describe a two-dimensional figure, shown in Figure 3-17. This tube is used for digital printing. Other types of tubes have a narrow band of wires which span the entire width of the tube, and are used for facsimile reproduction, the recording medium being stepped one line at a time.

The tubes developed by Litton's Tube Division have been intended for printing of highly detailed images, often for later projection. As a result, the development trend has been toward smaller and smaller wires, with the wire matrix surrounded by a metal head for control of capacitance. The best resolution measured to date is 230 line-pairs/inch, with ten grey scale steps. Calculations have indicated that 500 line-pairs/inch are achievable.

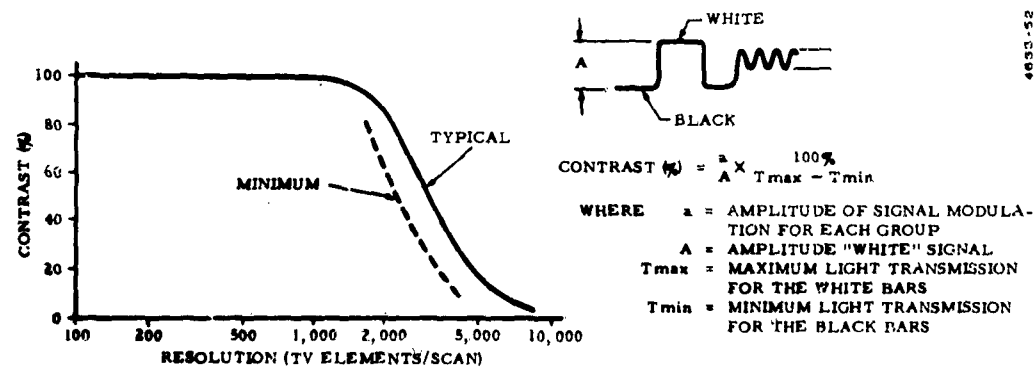


Figure 3-15. Line-Scan Tube Resolution

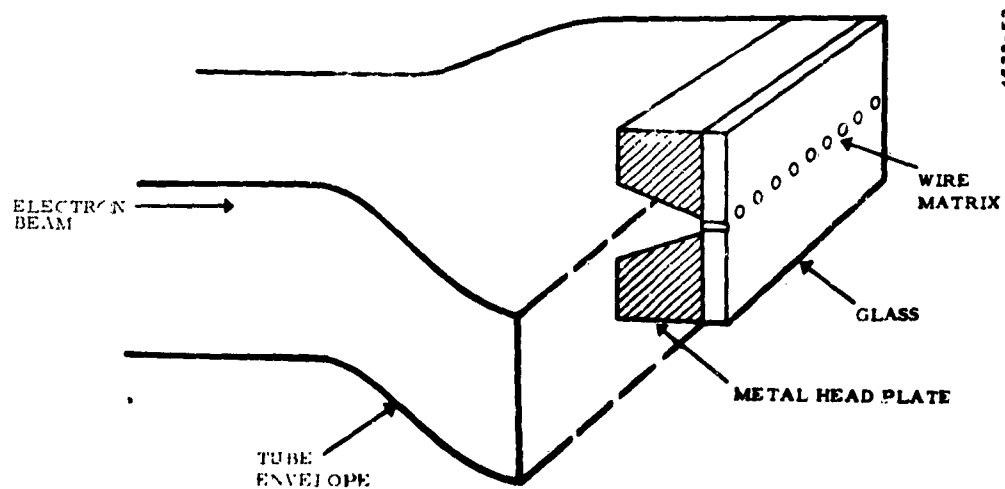


Figure 3-16. Electrostatic Discharge CRT (Sectionalized head)

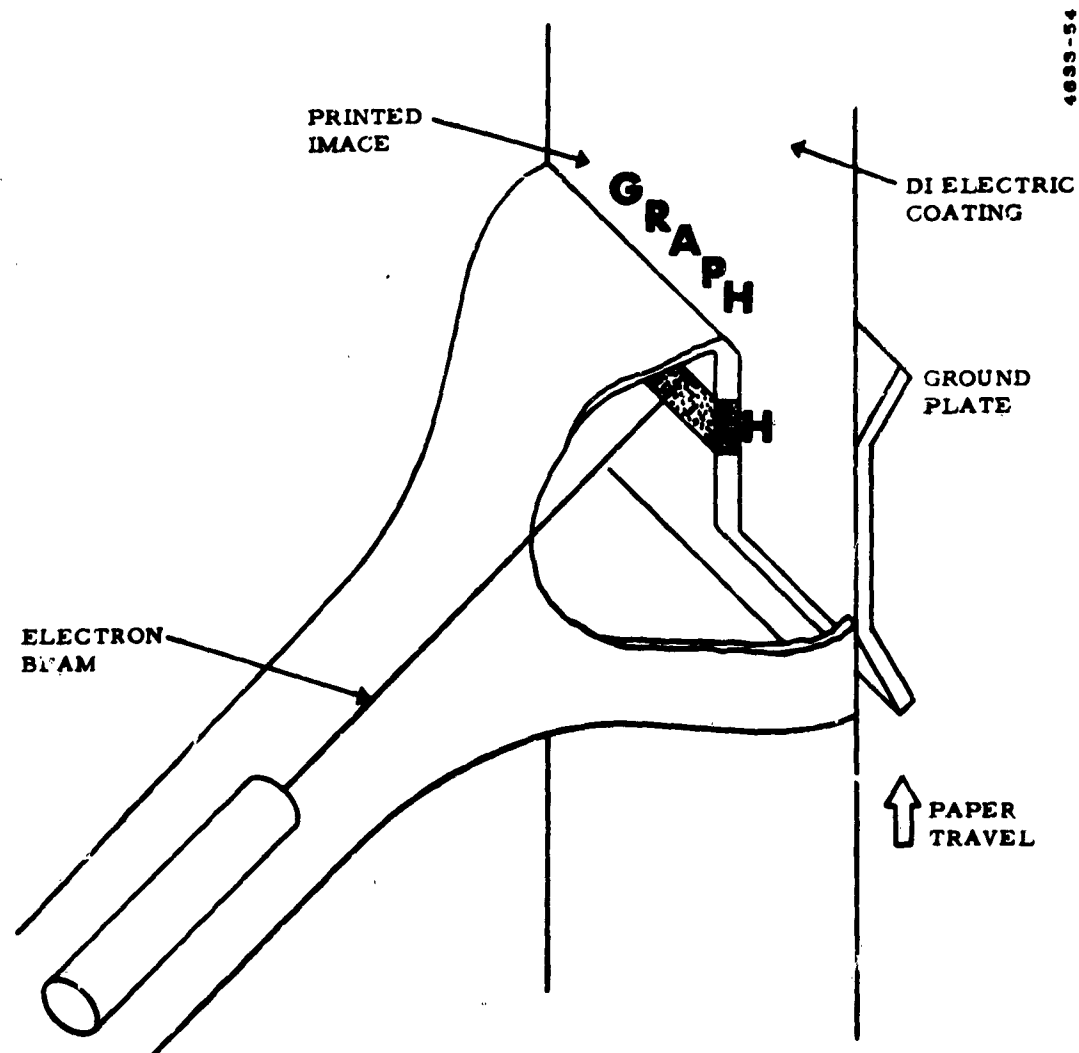


Figure 3-17. Two-Dimensional Wire Faceplate Electrostatic Discharge CRT

3.2.14 Storage Cathode Ray Tubes

Storage Cathode Ray Tubes and their relation to one another are depicted in Figure 3-18.

Storage CRTs -- Direct View:	Bistable Halftone Character Multi-Mode
Electrical Output -- Single Gun:	Barrier Grid Transmission Grid Modulation MTI Storage
Dual Gun:	Transmission Grid Modulation EBIC Fiber Optics Photon Transfer

Figure 3-18. Storage Tubes

Both types of storage tubes, Direct View and Electrical Output types, are extensively used. Direct view tubes are used in place of the conventional cathode ray tube when either persistence or high light output (such as might be required in an aircraft cockpit) is required; electrical output types are used for storage of data without display, the display cycle occurring later, and thus can be used for conversion from one time base to another time base for display. To achieve display persistence, then, either a direct view storage tube can be utilized, or a combination of conventional CRT paired with an electrical output type can be used to achieve the same result.

3.2.15 Electrical Output Storage Tubes

These are discussed in the section entitled Scan Conversion.

3.2.16 Direct View Storage Tubes

Direct View Storage Tubes have been extensively used in high light environment where the high light output of the storage tube is required. This feature of storage tubes has also permitted their use in projection systems.

There are two basic types of direct view storage tubes, the "halftone" and the "bi-stable". The halftone type permits a complete spectrum of gray shades to be displayed, while the bi-stable tube permits only one level of display; the halftone storage period is generally less than one minute, while the bi-stable is retained until intentionally erased.

A typical direct view storage tube is illustrated in Figure 3-19. All of the usual elements of a cathode ray tube are utilized, and the deflection can be either electrostatic or electromagnetic for the write gun. The phosphor screen of the conventional CRT is replaced by a storage screen, and a flood gun is added. The storage surface is comprised of an electroformed nickel mesh with dielectric on the side facing the electron guns. With the dielectric initially charged negatively with respect to the flood gun cathode, no electrons are permitted to pass through the mesh, and the screen appears black. When the writing gun bombards the dielectric with high energy electrons, secondary emission causes the storage mesh to become positively charged in the written areas, and the secondary electrons are collected by the collector mesh. Flood electrons penetrating the mesh in the charged areas are accelerated to the phosphor viewing screen, where they produce the light pattern corresponding to the charge pattern on the storage grid. Depending upon the potential to which the grid is charged, intermediate shades of gray ("halftones") can be achieved.

Since the flood electrons reproduce the charge pattern but do not regenerate it, the maximum retention time is limited; the maximum storage time for the tube operating in standard conditions is approximately one minute. Erasure, either instantaneous or a controlled gradual decay, can be effected by pulsing the storage electrode.

Degeneration of the charge on the storage mesh is caused primarily by the positive ions produced from residual gas molecules. In the bi-stable tube, the construction prevents the gradual erasure of the stored charge. A typical tube is shown in Figure 3-20.

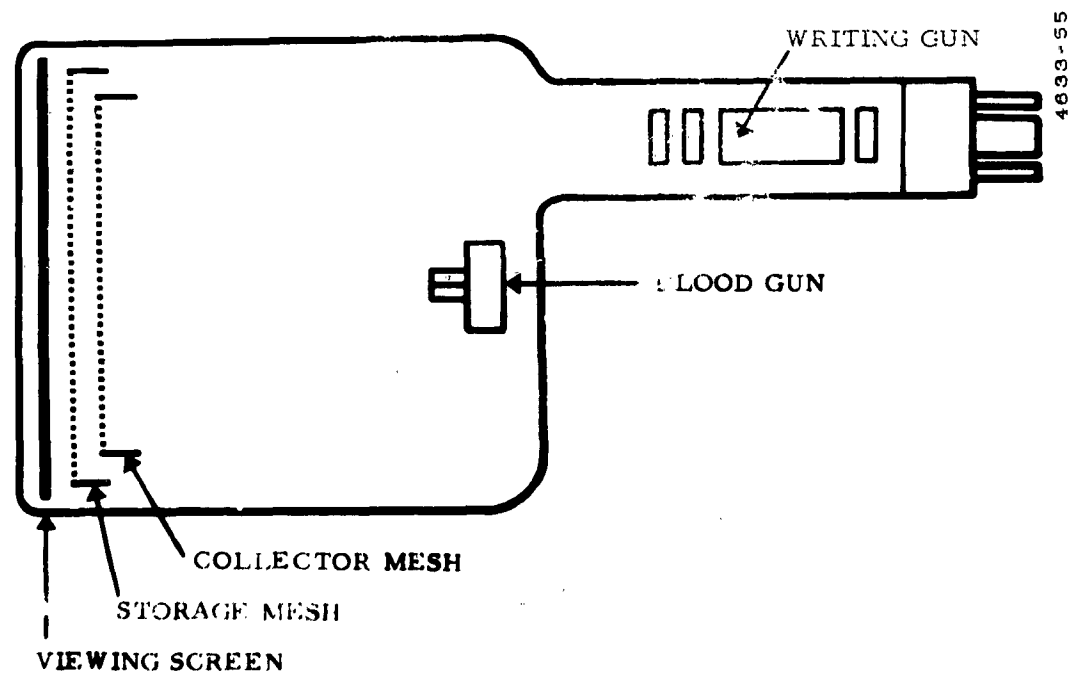


Figure 3-19. Halftone Storage Cathode Ray Tube

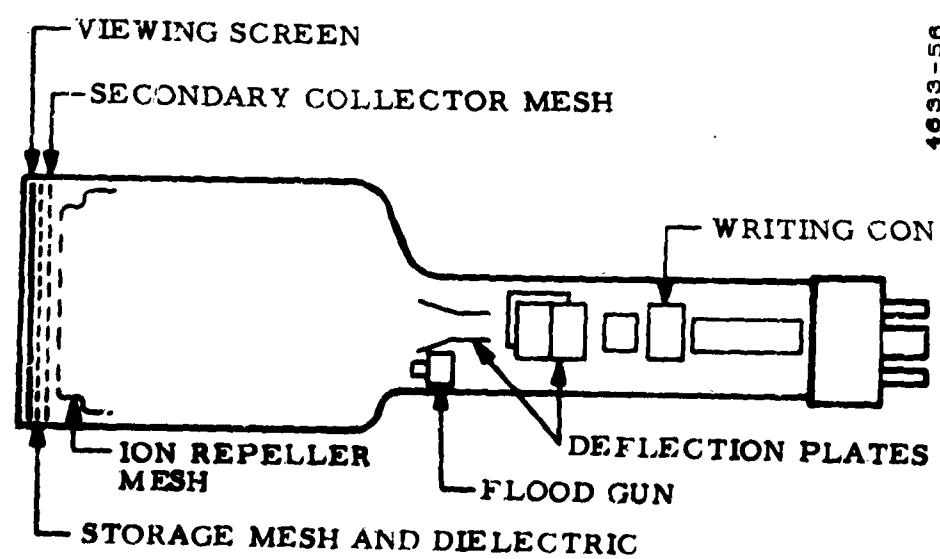


Figure 3-20. Bi-Stable Storage Cathode Ray Tube

A modification of the basic bi-stable storage tube is the Typotron, made by the Hughes Aircraft Company. This tube incorporates beam shaping character matrix, as described in the section on beam shaping tubes. This tube is illustrated in Figure 3-21. The desired character is selected by applying the proper voltage to the selection plates. The convergence coil inverts the image of the character and focuses it on the storage screen. Compensation plates redirect the image along the tube axis and between the deflection plates, which are then used to position the image at any desired place on the tube face. A flood gun covers the entire screen with a barrage of low velocity electrons to produce a bright visible picture.

Direct view storage tubes have been made in many different sizes, the most typical size being 5" and the largest is the Hughes 21" Tonetron. The maximum size is limited by the difficulties in achieving beam collimation and retaining beam density over large areas.

A new development in direct view storage tubes is the multimode type, illustrated in Figure 3-22. This tube permits selective erasure of any part of the display, presenting stored and nonstored information simultaneously, and displaying high contrast, high resolution information in either dark or light trace modes. The multimode tube operates in much the same way as a conventional storage tube, except that it additionally employs "bombardment induced conductivity" effects, in addition to secondary emission.

The stored data of the multimode tube is written on the storage mesh with a relatively low energy writing gun beam. Then, by using a high energy erase gun, a selected portion of the mesh can be erased through the following process: the target dielectric is made conductive by bombardment, and the effects of secondary emission is overwhelmed. Charges stored on the dielectric surface are thus discharged to the backing electrode, causing erasure of those areas. At intermediate levels of energy, writing and erasing effects cancel, enabling presentation of nonstored and stored information without disturbing the stored data.

Many arrangements of guns are possible, from using one gun for both write and erase and switching energy levels to using separate guns, to use of multiple guns. By placing the entire storage mesh in a charged condition, and writing on it with the erase gun, a high contrast, black on white display may be presented. By modulating the erase gun to vary current as the mesh is scanned, halftones can be generated.

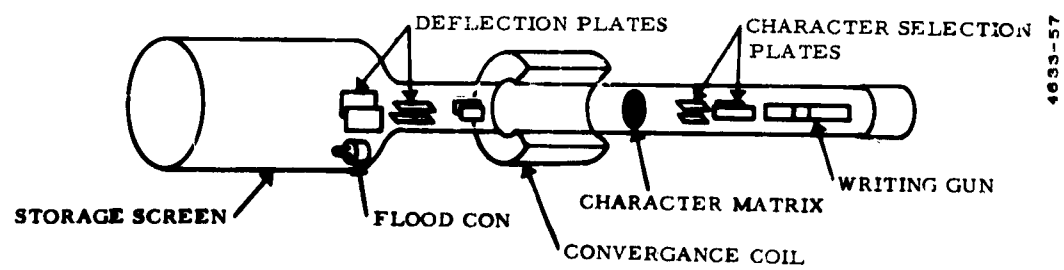
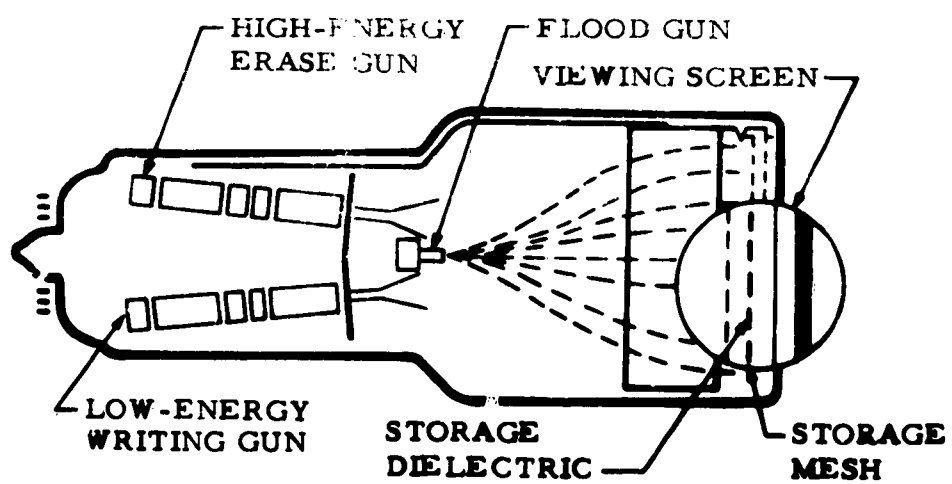


Figure 3-21. Typotron Storage Cathode Ray Tube



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Figure 3-22. Multi-Mode Storage Cathode Ray Tube

Typical storage tube operation is: Brightness 200 to 4000 foot lamberts
Resolution 50 to 100 lines per inch
Writing Speed 300 to 300,000 inches/
second
Halftones at least 5 distinguishable
levels

Storage cathode ray tubes are much more complex than conventional cathode ray tubes, and hence much more expensive; as a comparison, a conventional 5" CRT costs no more than \$50, while a storage tube of this size can cost \$1,000 or more. Because of the numerous voltage required, and the added functions of erasing and flooding, the electronic equipment required for operation of the storage tube is much more complex than that required for a conventional display. Even with these drawbacks, together with poor resolution, storage tubes are required for operation in high ambient light conditions; they are, for example, extensively used in aircraft displays.

3.2.17 "One of a Kind" Cathode Ray Tubes

Several cathode ray tube devices have been developed which do not logically fit into any of the categories listed for Cathode Ray Tubes, either because of their design or their experimental nature. Typical of the first category are Cathode Ray Switch Tubes; typical of the second is the Composition CRT, which converts a character image into formed beam pattern.

Beam switching tubes take advantage of the inherent high speed switching possible with an electron beam to make a selection from multiple contacts; such a tube is illustrated in Figure 3-23. Aluminum targets are deposited on the surface of the header, and the electron beam is deflected to the desired target with the electrostatic deflection plates. Thus, any one of the targets can be selected ("switched"), either sequentially or randomly. The typical switch tube has ten elements, although units have been built with up to 256 elements.

A traveling image CRT has been developed by the Raytheon Company. Referred to as TRIST, this tube will produce a continuously moving map-like display of data, for airborne reconnaissance and observation in real time. This CRT is shown in Figure 3-24. A 4" wide endless belt of stainless steel foil, coated with a scotophor of potassium chloride, is stretched between a pair of parallel rotating drums. This produces a

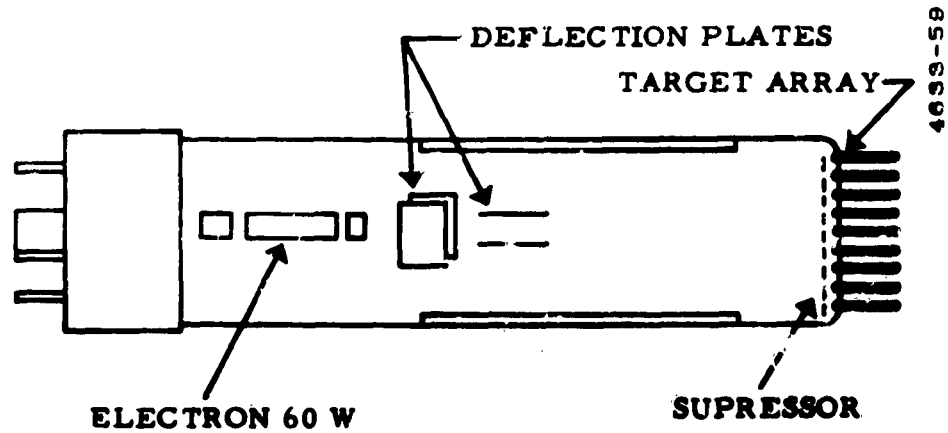


Figure 3-23. Cathode-Ray Switch Tube

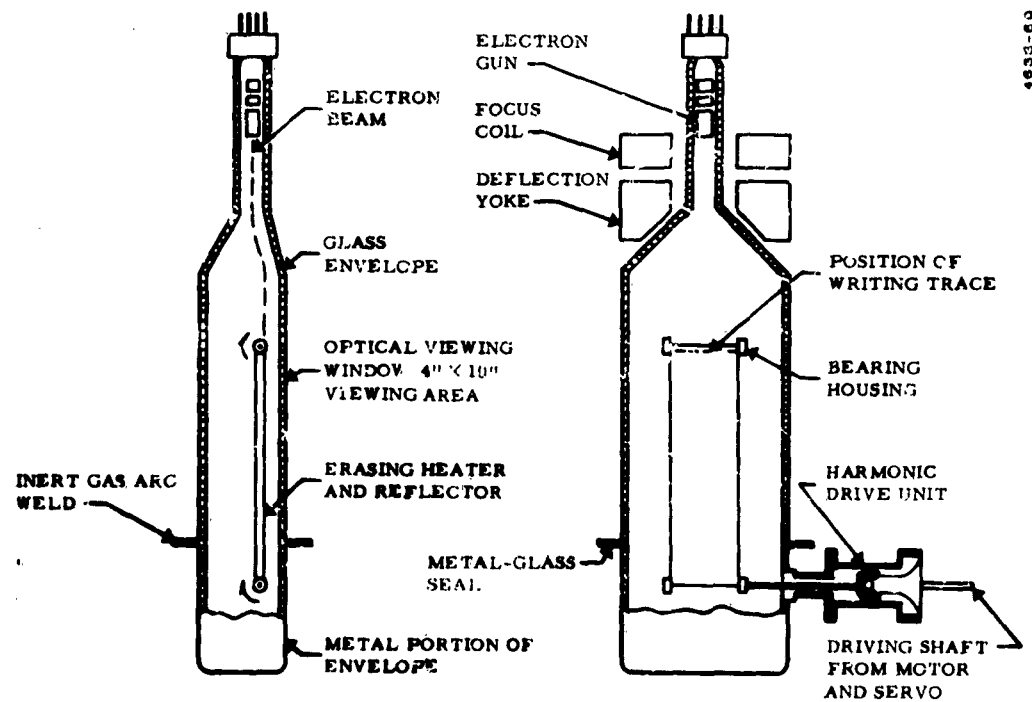


Figure 3-24. Trist Traveling-Image Cathode Ray Tube

10" long viewing surface. The signal is inscribed on the long persistence scotophor by the electron gun, the display then moves down the face of the tube as the belt turns, and a moving display is thus generated. As the belt goes around the second drum, out of view, it is heated and the signal is bleached.

The Composition Cathode Ray Tube is illustrated in Figure 3-25. Unlike the beam forming CRT's discussed earlier, like the Charactron, where the electron beam is formed by directing the beam through a shaped aperture, the Composition CRT starts the process from a film chip or slide. The character matrix of the film chip is projected onto the photoemissive cathode using a projector. The photoelectrons are emitted as shaped beams, are focused on the selection aperture, and the desired character is directed through the aperture by the deflection selection coils. This character is then treated as a convention electron beam, deflected to the desired point on the screen for display.

Undoubtedly, many other special purpose Cathode Ray Tubes can be devised to take advantage of the flexibility of the electron beam; these are merely several of the various applications of the Cathode Ray Tube.

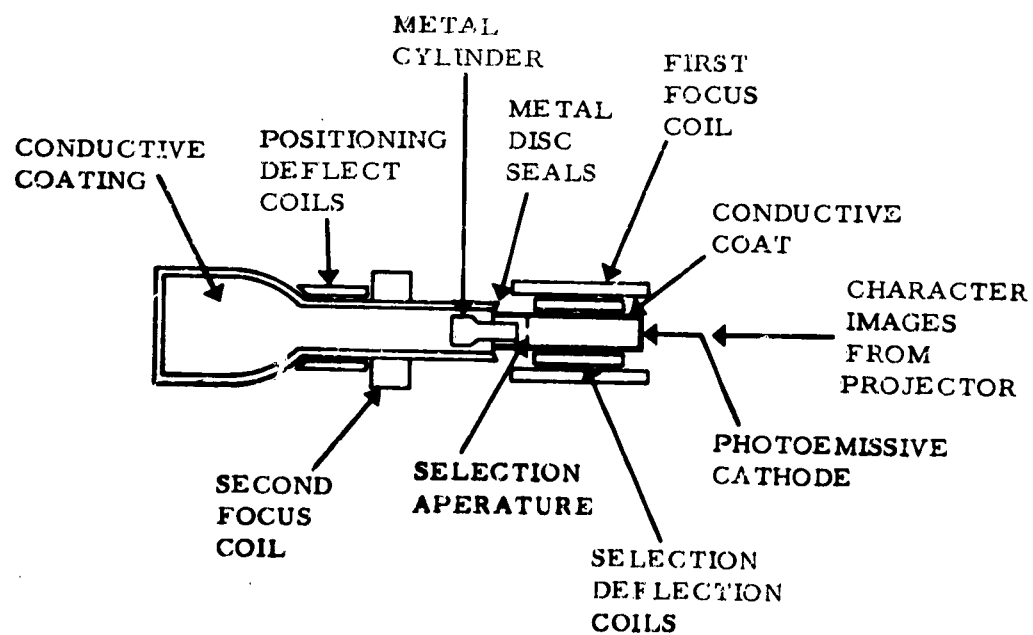


Figure 3-25. Composition CRT

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3.3 SCAN CONVERSION

Scan conversion is finding increased application in avionic display systems due to recent improvements in performance characteristics and ruggedization as well as reduced weight and volume requirements. Basically, scan conversion is the recording of sensor information in its raw data format and its conversion to TV video. It is thus an electrical input to electrical output conversion. The output TV video from the scan may be displayed on an ordinary TV monitor. A block diagram of a scan conversion system is shown in Figure 3-26.

The essential components of a scan converter tube are: a) one or two electron guns; b) a storage target to store the instantaneous raw video; and c) a collector which gathers the secondary electrons representing the TV video produced during the reading operation. In single gun scan converter tubes, the gun is sequentially time shared to perform the "writing" of the sensor video and its subsequent "reading". Two gun tubes permit simultaneous and independent writing and reading. In addition, other major tube characteristics may be differentiated such as target structure, performance characteristics (storage time, resolution, cancellation ratio), and electrical and physical parameters. A major part of this review will be devoted to the different types of scan converter tubes.

3.3.1 Advantages of Scan Conversion

The potential advantages offered by scan conversion to avionics display systems includes the following:

1. Conversion of sensor data, including radar, infra-red, etc. to a bright, flicker free display on a CRT monitor.
2. Adjustable storage of sensor data for periods ranging from seconds to one-half hour. This feature is of particular importance in tracking situations, permitting the display of target trails with natural fade characteristics.
3. Signal integration to enhance target signals obscured by noise.
4. Direct signal cancellation of ground clutter as in MTI (moving target identification).
5. Ability to intermix sensor video and synthetic video derived from a digital computer, contour maps, sketches, etc.

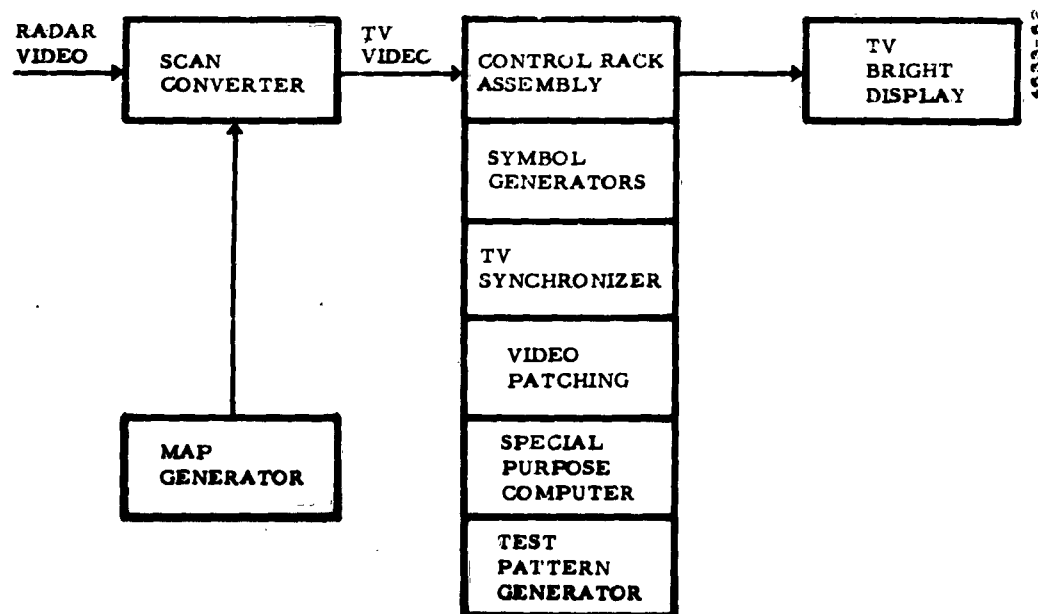


Figure 3-26. Simplified Block Diagram for Scan Conversion System

6. Selective or complete erasure of stored video by computer or operator command.

With the exception of item 4, which requires a special scan converter tube design, these characteristics may all be obtained from a single device.

Scan conversion also has an important resolution advantage as compared to direct view storage tubes (DVST). This is a direct result of the low beam current requirement, resulting in lower spot size. At current state of the art of electron gun design, the DVST has 350 lines/diameter in a 7 inch size while the scan converter tube typically has in excess of 1000 lines at target diameters on the order of 2.5 inches.

3.3.2 Theory of Operation

Scan conversion is based on: 1) the principle of electrostatic storage of electrical video on an insulating surface (which characteristic has long been available in TV pickup tubes); 2) the ability to "read" the stored video without destroying it.

Storage of signal occurs as electrostatic energy either by the deposition of electrons on the insulator (the target), or their removal through the phenomenon of secondary emission. As is well known, both metals and insulators exhibit secondary emission if bombarded by an electron beam sufficiently in excess of the surface material work function. For many materials this occurs at incident electron energies greater than 20 electron volts. The ratio of secondary electrons emitted to incident primary electrons is called the secondary emission factor K:

$$K = \frac{\text{secondary electrons}}{\text{primary electrons}}$$

K is a function of the target material and the incident beam energy (determined by the potential difference between the cathode and the target). For an insulator the approximate variation of secondary emission factor with accelerating potential is shown in Figure 3-27.

Two critical potentials, V_{c1} and V_{c2} , are shown in the figure. Low velocity primary electrons experiencing accelerating potential less than V_{c1} produce less secondaries than are contained in the primary beams ($K < 1$). In tubes designed primarily for scan conversion, this region is

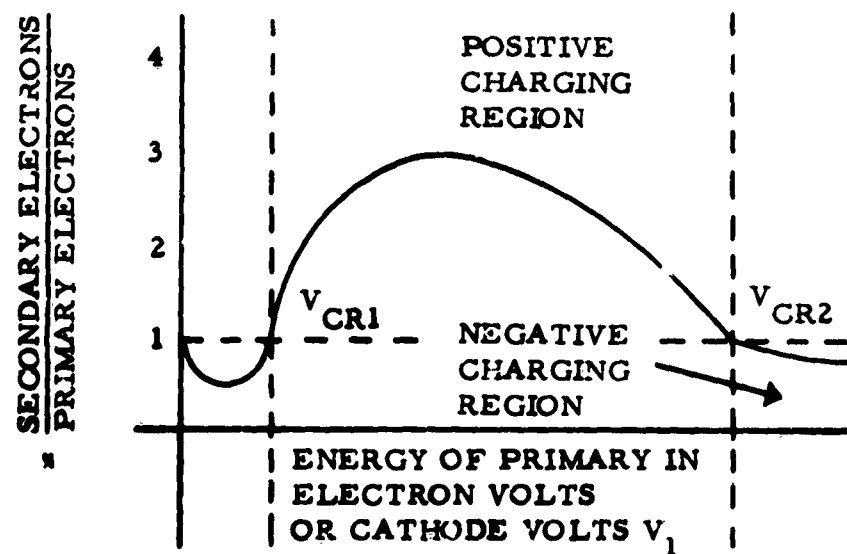


Figure 3-27. Secondary-Emission Ratio

used for erase/prime and reading operations (erase/prime consists in bringing the storage surface to a uniform potential, thereby erasing any previous written signals). In all scan converter tubes, writing is accomplished at acceleration potential such that K has an approximate value of 2 or greater (i. e. two or more secondaries produced for each incident primary electron). This occurs somewhere in the range $V_{c1} < V_{\text{accel.}} < V_{c2}$.

Figure 3-28 shows schematically one form of single gun scan converter. The signal to be written is applied to the electron gun control grid, while the beam is scanned across the target in the desired pattern. The overall writing process is linear because both the control grid characteristic of the electron gun, see Figure 3-29, and the target characteristics (charge density vs. beam current) are linear.

The target system used in scan converters has features not found in the previous television type pickup tubes. While these are not found in the various scan converter designs with the same physical embodiment, nevertheless the objectives remain the same:

- a. Prevention of redistribution of the secondary electrons which would make any comparison from scan to scan impossible.
- b. A further refinement to the above such that the reading beam does not come in contact with the stored charge. Thus multiple reads of the same signal may be obtained with little degradation effects.

Feature a. was first accomplished in tubes with high beam energy and secondary emission ratio greater than unity through the so-called barrier grid used in the Barrier Grid Storage Tube. Feature b. was accomplished by converting the target to a mesh, enabling the read electron beam to reach the collecting anode without impingement on the target. This feature was provided in a later designed tube now called the Transmission Grid Modulation Tube. These features will be described in a later section concerned with a description of the different tube types.

3. 3. 3 Types of Scan Converters

All scan converters are alike in that they are designed to accept input video data in electrical form and to provide output video data in electrical form (usually TV raster format). Scan converters may be differentiated

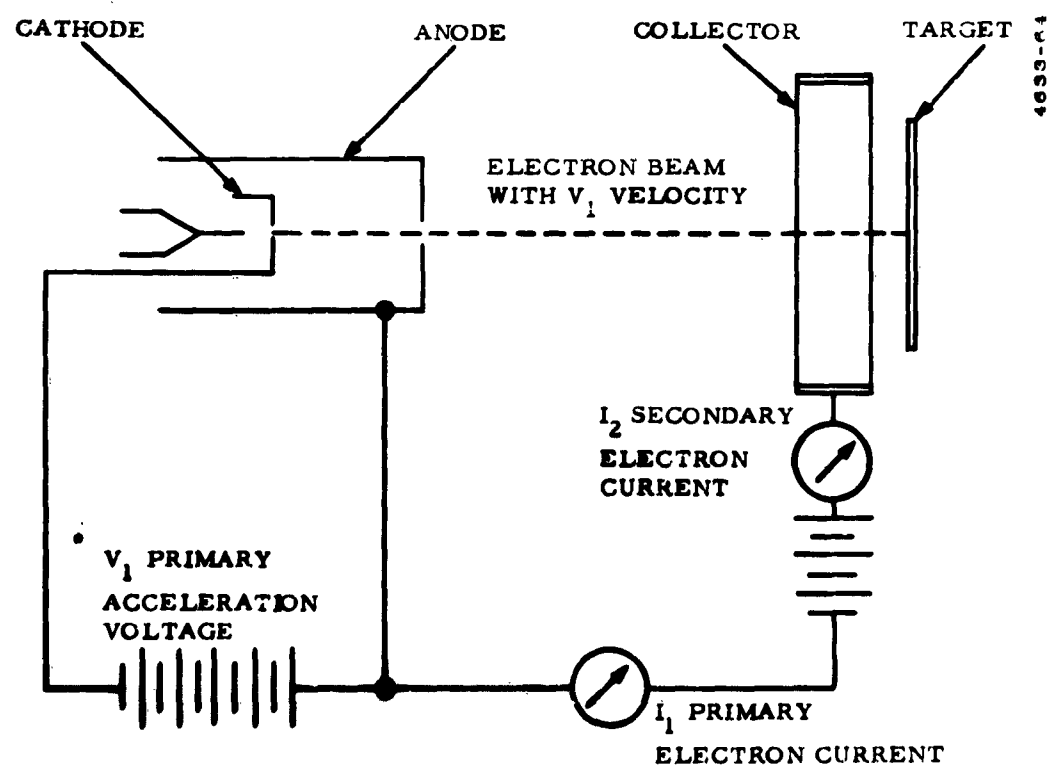


Figure 3-28. Schematic of a Secondary-Emission Target System

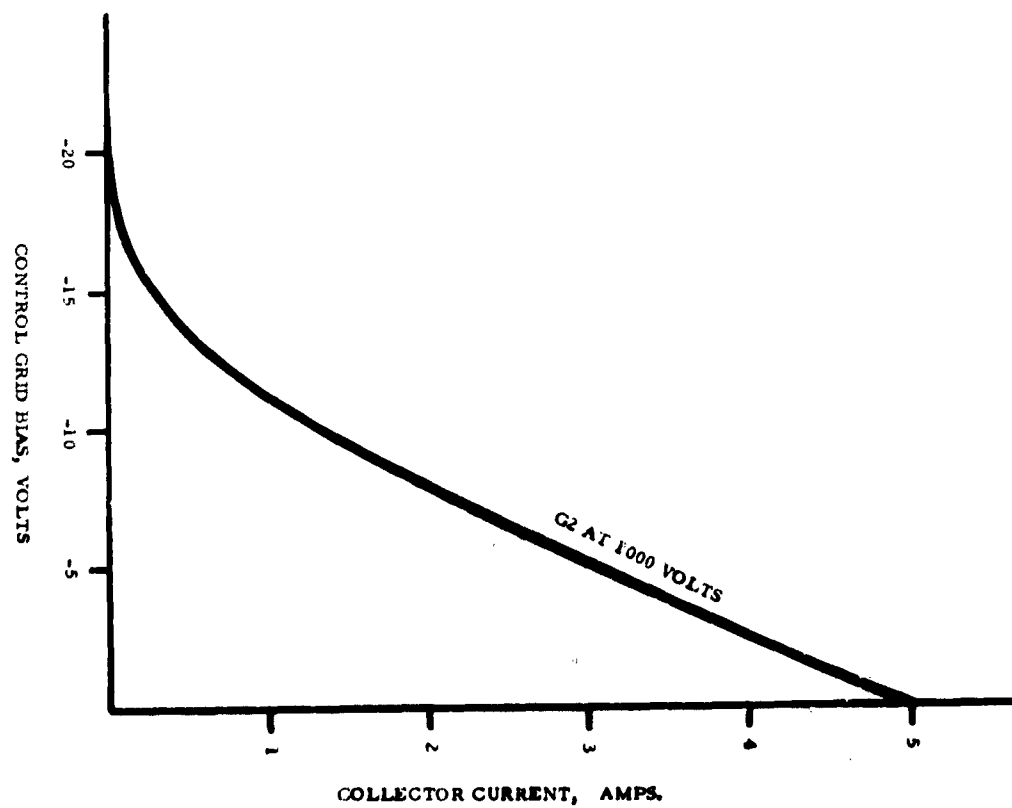


Figure 3-29. Control-Grid Characteristics
of Scan-Conversion Tube

by two principal construction features: The number of electron guns (single or dual) and the storage target structure. A classification including the major types of scan converters is the following:

Single Gun

1. Barrier Grid
2. Recording Storage Tube
3. MTI (Moving Target Indicator) Storage Tube

Dual Gun

1. Transmission Grid Modulation
2. EBIC (Electron Bombardment Induced Conductivity)
3. FOPT (Fiber Optics Photo Target)

In single gun scan converters, the electron gun is sequentially switched through a three step cycle as follows:

1. Erase/Prime (performed separately or combined)
2. Write input video on storage target
3. Readout stored video in TV raster format

In a dual gun tube, priming and writing are accomplished as in the single gun tube. However, the reading operation may be performed simultaneously with these operations, resulting in greater flexibility of operation. Another advantage is that automatic or gradual priming is possible without the necessity for switching any electrode potential. In this manner, varying target trail decay rates may be selected and, in addition, mode switching completely eliminated. The principle cost is in greater complexity of the basic scan converter since two guns must be provided, and also a length penalty of nearly two to one resulting from the fact that the write and read guns are displaced on opposite sides of the storage target. A possible operational difficulty is cross talk noise induced through simultaneous operation of the write and read beams. This has lately been reduced to unobjectionable levels through such techniques as frequency separation of the write and read beams by RF modulation of the latter; video cancellation; and more recently, improved target structures having inherently low cross talk susceptibility.

3.3.4 Single Gun Storage Tubes

Barrier Grid

The barrier grid storage tube exemplifies the class of tubes using a grid or screen near the insulating surface to prevent the return of secondary electrons to the insulating surface. This tube has been applied to a variety of uses including image storage, scan conversion, background cancellation for area MTI, and binary information storage with random access.

Figure 3-30 illustrates the construction of the barrier grid storage tube. The three basic assemblies are:

1. Electron Gun and Primary Optics
2. Target Assembly
3. Secondary Optics

The electron gun may be of the triode or tetrode type and consists of a cathode, grid, and anode(s). Typical operating potentials are

cathode	-1000 to -2000 v
grid	100 v below cathode voltage
anode	-150 v relative to ground

The high cathode voltage requires a heater transformer having a minimum insulation rating of 2500 v. Focussing and deflection may be magnetic or electrostatic, the latter being illustrated. Overall resolution of the electron gun and primary optics assembly is such as to produce a 3-mil spot with a beam current of 5 a and drive of 30-70v.

The target assembly is a three layer sandwich consisting of the metallic barrier mesh, a sheet of mica dielectric (sometimes sprayed with an emitting material), and a thin metallic backplate. The target assembly is in effect a continuum of elemental capacitors formed by elemental areas of the dielectric and the plate and barrier grid. Figure 3-31 shows a cross section of the target assembly. Equivalent capacities are shown in Figure 3-32 and are of the following magnitude: $C_s \approx C_p = 200-4000$ pf; $C_L = 5-10$ fp; $C_{coll} = 8-12$ pf. With respect to mesh fineness, a

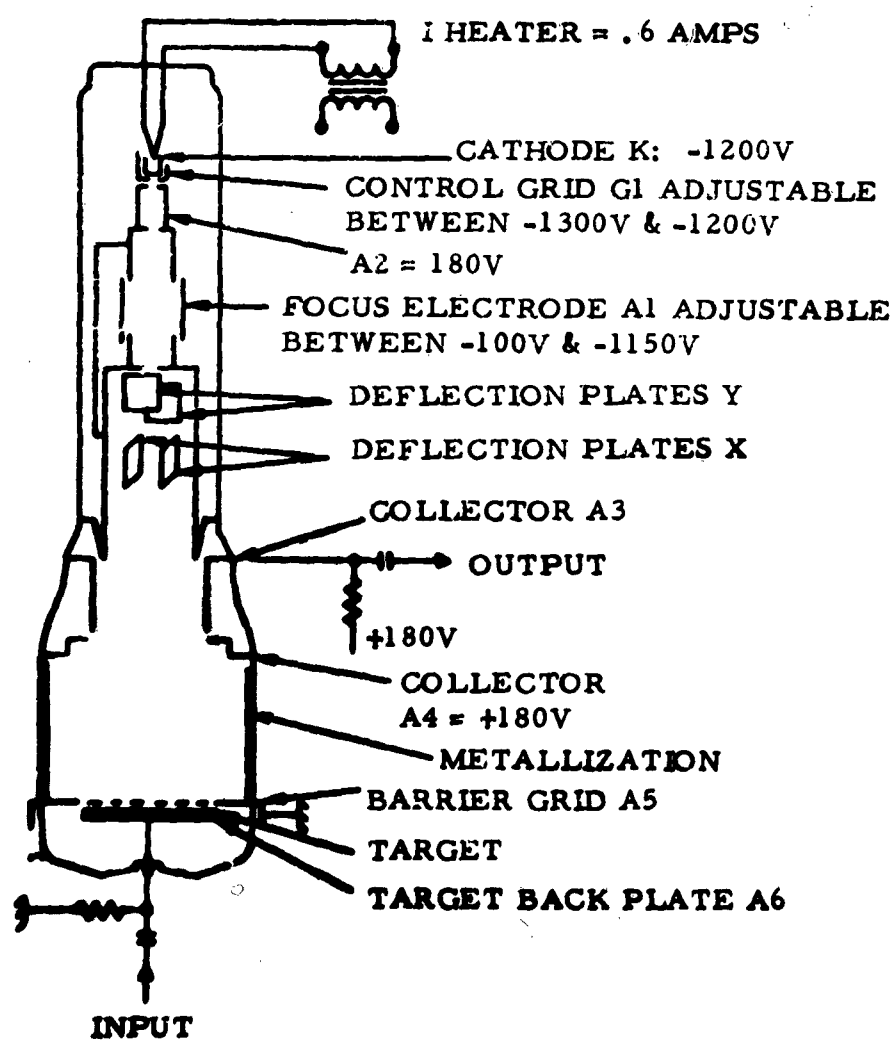


Figure 3-30. Barrier-Grid Storage Tube

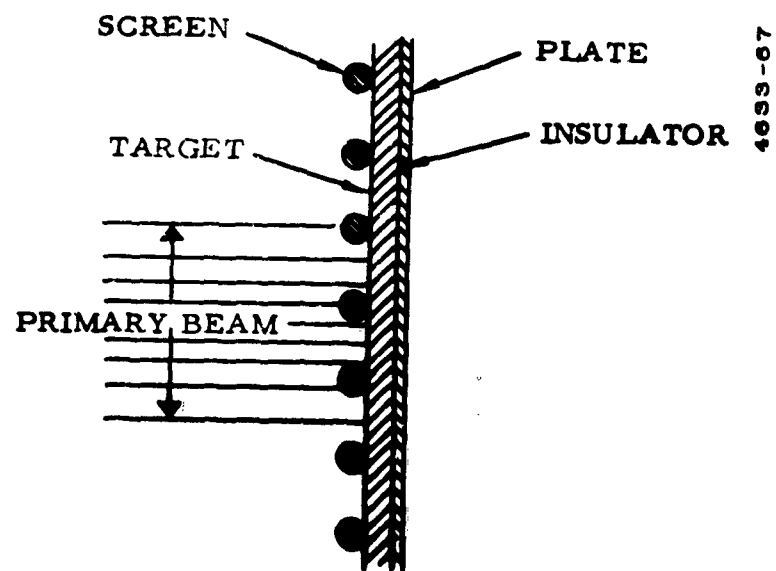


Figure 3-31. Target Structure

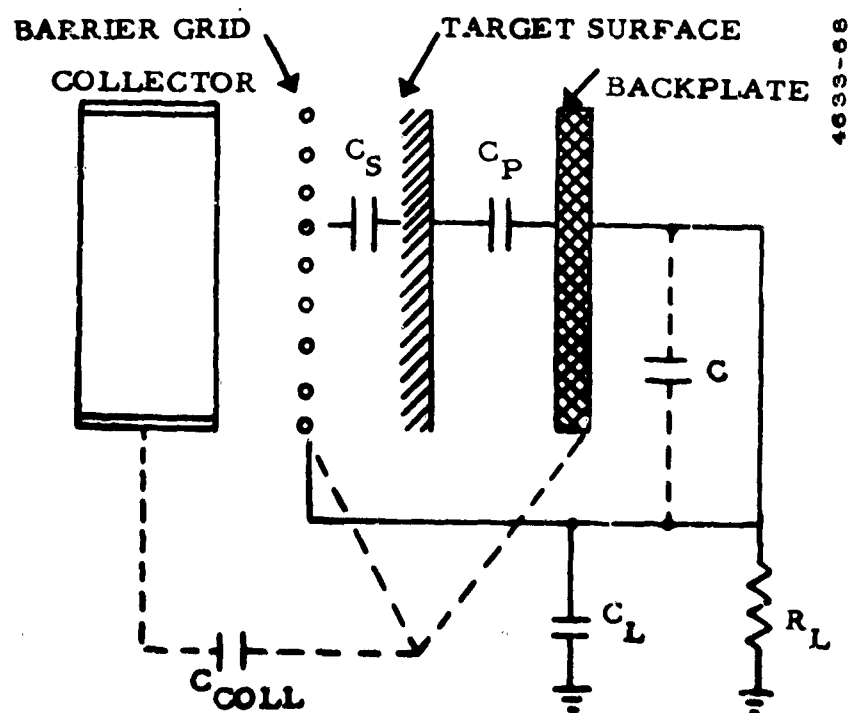


Figure 3-32. Target Capacities of Barrier-Grid Tubes

compromise is required between optimum barrier grid localization of secondary electrons during write and the problem resulting from interception of secondary electrons during the read operation.

The secondary optics is comprised of the collector which serves to collect secondary electrons. As illustrated in Figure 3-30, it is a cylindrical electrode close to the target. The secondary electrons must be collected uniformly to prevent signal distortion by frequencies synchronous to the scanning pattern.

Operation: Operation of the barrier grid tube is in a three step cycle: Write, Read, and Erase and Prime.

- a. To write, the backplate is set at +25 to +50 volts, the barrier grid is at ground potential and the collector is at +150 volts. The electron beam modulated by the input video scans the target depositing a charge pattern, varying in intensity, that is a linear reproduction of the time variation of the impressed signal.

The beam acceleration potential is such as to produce a secondary emission ratio equal to about two. A quantity of secondaries just equal to the number of arriving primaries penetrate the barrier grid and are collected by the collector. The remaining fall back to the screen and are prevented from redistributing through the action of the barrier grid. From the foregoing it is seen that during the writing phase, the signal will appear on the collector as a modulation of the secondary beam.

- b. To read, the backplate is switched to zero volts, and the barrier grid and collector are maintained at the same potentials as for writing (0 volts and +150 volts respectively). This has the effect of removing the charging voltage from the plate and also of returning all parts of the target not written onto to the equilibrium potential. The portions of the target that have been written upon are negative with respect to the equilibrium potential by the potential distribution through which they were discharged during writing.

The unmodulated writing beam scans the target, again with an energy such that the secondary emission ratio is greater than unity. The escaping secondaries constitute a current which has a time variation in accord with the charging voltages of the elemental target area on which the scanning beam is impinging. This varying secondary current is collected at the collector and develops an output video signal across the collector capacitor. As a result of the reading process, the target is charged toward the equilibrium potential.

- c. **Erase and Prime** - The backplate is switched slightly positive with respect to the barrier grid. The unmodulated electron beam scans the target as in reading, bringing the target to the equilibrium potential. In some applications, erase and prime are not required in as much as reading is also an erasing action. This is dependent on the discharge factor of the tube which is the ratio between the voltage difference through which the target capacitance has been discharged by one passage of the beam and the target's initial voltage difference from equilibrium.

$$F = \frac{V - V_b}{V}$$

where f = discharge factor; V = charging voltage applied to target, the initial potential difference of target from equilibrium; V_b = potential difference of target from equilibrium after one passage or application of beam.

Recording Storage Tube

The single gun RST has been employed both as a recording storage tube and as a scan converter. The RST, illustrated in Figure 3-33, is similar to the barrier grid both in its operational characteristics and structure. However, it differs in the specific details of the electron gun, electron optics, and target assembly.

1. Electron Gun and Electron Optics

Production versions of the RST such as the CK 6835/QK 464A employ a triode gun with elements consisting of a cathode, control grid, and anode. Higher resolution types have employed a tetrode gun configuration.

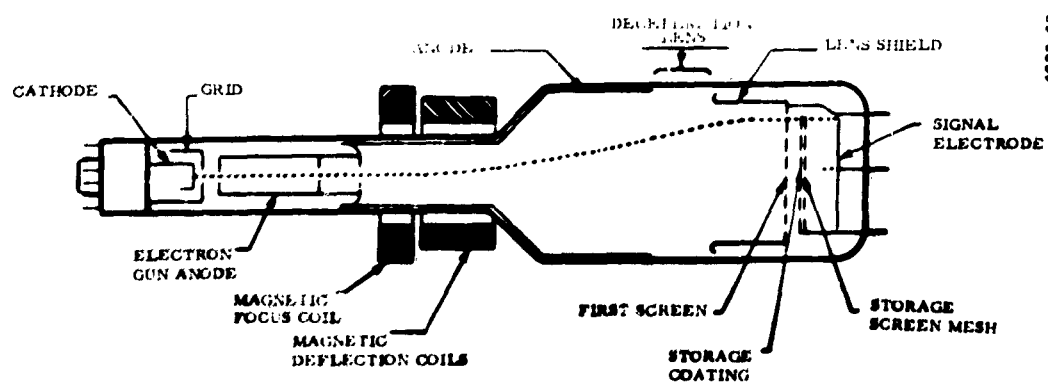


Figure 3-33. Schematic Drawing -- CK-6835/QK-464A

Focusing is accomplished using an electromagnetic focusing coil similar in design to commercial television focus coils. However, a special feature is the use of homogeneous Swedish iron in the shell to minimize astigmatism. Deflection is also electromagnetic. If both the input video and output video are in TV format, a commercial television deflection yoke can be used. However, if the input is PPI at slow rates as in radar, and the output is TV raster, a special yoke design is required.

The variation in angle of arrival of the electron beam at different locations on the target causes undesired variations in the writing of information. This effect is avoided by the collimating lens system comprised of the anode coating, lens shield, and decelerator screen. The passage of the electron beam through the lens causes it to strike the target at right angles regardless of the initial deflection angle.

2. Target Assembly

This is comprised of the storage screen and the collector. The storage screen is a woven metal screen with 600-1000 wires per linear inch and coated on the electron gun side with a dielectric such as calcium dioxide. The coated metal mesh has the appearance as shown in Figure 3-34.

The collector serves to collect the output signal current during reading. The electron beam forming the output current is that portion of the primary beam passing through the apertures in the storage screen.

3. Operation

As in the operation of the barrier grid tube, the RST is cycled through the write, read, erase/prime modes through control of target electrode voltages. In the RST, the storage screen potential is the primary controlled quantity. The operating modes as a function of storage screen potential are summarized in Figure 3-35.

- a. **Write:** The storage screen is set to +300 volts. At this voltage the secondary emission ratio is on the order of two to three. The dielectric surface tends to charge to the +300 v level and would do so if a constant amplitude beam current of sufficient magnitude were used. The beam however, is modulated by the incoming video, and thus the screen is not at a uniform potential but at a potential which varies with the amplitude of the modulated beam. The voltage level varies between 270-300 volts.

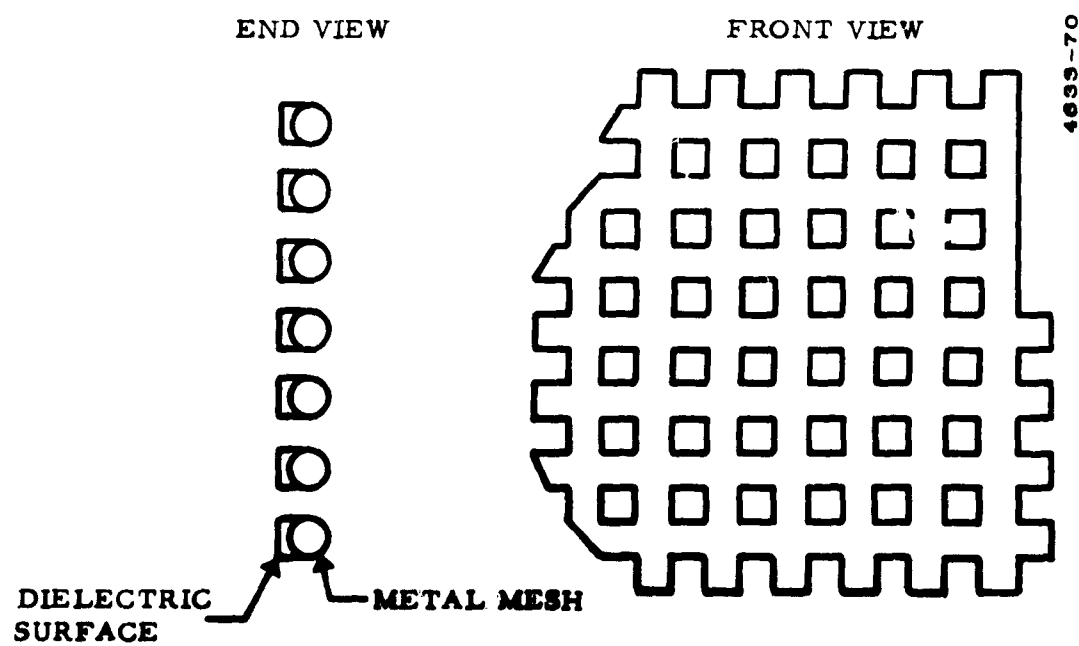



Figure 3-34. Storage Screen

MODE	STORAGE SCREEN	DIELECTRIC SURFACE
PRIME (ERASE)	30V	30V 0V
WRITE  (INPUT SIGNAL)	300V	270V ↓ 223V ↓ 300V
READ (ASSUMING -13V = CUT-OFF)	17V	-13V ↓ 0V ↓ +17V

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Figure 3-35. Storage-Tube Operating Modes

- b. Read: The storage screen potential is set to +17 volts, well below the critical potential V_{c1} . The dielectric surface follows

this potential charge, maintaining the written-in potential differences. As a result, the dielectric is now actually negative with respect to the cathode (cathode at ground potential). The collector is highly positive with respect to the storage screen.

As the unmodulated electron beam scans the target, it is modulated by the negative variational electric field. The modulated beam passes through the apertures of the storage screen and is urged into the collector by the high collector-screen potential difference. Because the read beam tends to pass through the storage screen without incidence on it, the reading is non-destructive and multiple readouts can be effected (this is not the case with the barrier storage tube which actually was designed to effect nearly complete erasure upon performing the reading operation).

The variation of potential of the insulating surface during write and read is of interest. While the target screen is at +300v during write, the storage screen only charges, say to 284 volts even at the peak amplitude of the modulated write beam. The lower limit is on the order of 270v which corresponds to the weakest signals to be written. Now when reading is to occur, the storage screen is switched to +16 volts. Thus, points on the insulating surface which had a voltage of 284 V are now at zero volts. If, however, the writing signal was such as to generate to maximum voltage higher than 284V, the storage screen, functioning like a positive driven control grid, would clip the peaks to zero volts.

On the other hand, signals which were written at +270V now correspond to -14V. The minimum signal to be read should just correspond to the cutoff point of the screen, i. e., the potential below which no current passes through to the collector. When the upper and low limits of the input signals are so written, the optimum dynamic range of the storage tube is obtained (maximum shades of grey and maximum signal to noise ratio).

- c. Priming: The storage screen is set to +30V, which is less than the critical voltage (V_{cl}). The dielectric charges to the cathode potential (0 volts) as it scanned by the unmodulated electron beam. Previous stored information is thereby erased and new data may be entered.

Automatic priming, that is, destructive readout can be achieved through selection of the proper reading beam energy and the collector potential. As these are lowered, less energetic electrons are reflected back to the storage screen thereby causing destruction of the stored charge image.

MTI Storage Tube

A measure of the fidelity of reproduction of one of the first storage tubes, the barrier grid, is the "cancellation ratio". The cancellation ratio is derived by comparing the reproduced signal with the original by subtracting one from the other. Any residual signal would be a measure of either phase or amplitude distortion or both. The particular advantage of this procedure is that it is accomplished entirely within the tube.

The cancellation process is accomplished as follows. The input signal does not modulate the electron beam but is applied instead to the back-plate. The unmodulated electron beam, scanning the target, deposits on the insulating surface a charge pattern varying in intensity with the time variation of the impressed signal (which acts as a time varying charging potential). During the process the signal will appear on the collector as a modulation of the secondary beam.

Now, assume the same signal is applied on successive scans, as would be the case for fixed target radar video. On the very next scan, no additional charge will be deposited by the unmodulated beam, since the charge is still on the storage surface. This is also the case for succeeding scans as there is no change in the applied signal. As a result, the secondary beam originates from a target now at equilibrium potential and therefore will be constant.

A modern MTI storage tube is shown in Figure 3-36. Its size, similar to a TV vidicon pickup tube, is only 1" diameter by 6" in length. While the illustrated tube uses electrostatic focusing and deflections, other types have used magnetic for higher performance. The electron gun is of conventional design. Acceleration voltage of 300-400 volts is required.

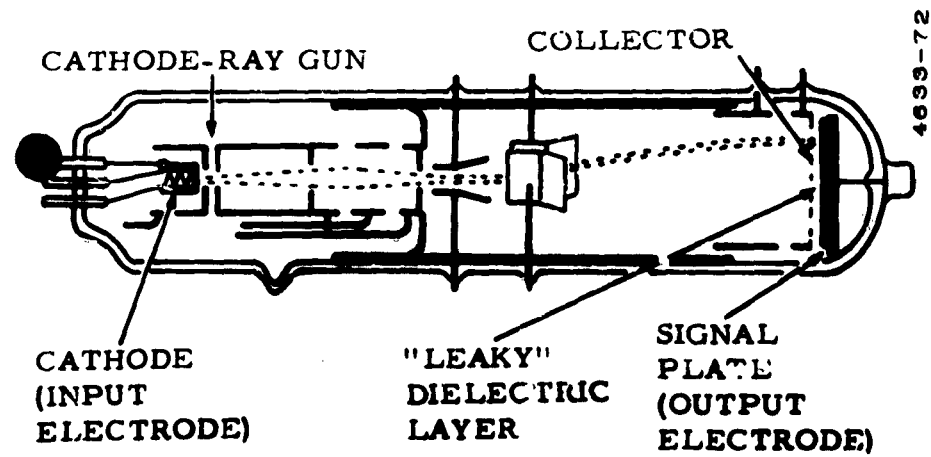


Figure 3-36. MTI Storage Tube

The target structure of the MTI tube shown has a solid dielectric and backplate target structure as in the barrier grid tube; however, the barrier grid itself has been removed. The collector is in front of the storage surface.

1. Performance: Cancellation ratio from 50: 1 to 300: 1 may be achieved according to the desired resolution. The cancellation time may be varied from 1 to 10 scans. A wide range repetition rates may be accommodated varying from TV rates down to 60 seconds/scan. Resolution is on the same order as commercial TV, ie 250×250 elements per picture.

Application of Single Gun, Non-Viewing, Storage Tubes

Figure 3-37, from reference 5 shows the application of available non-viewing single gun storage tubes to scan conversion, storage, and MTI. While the chart omits the date, target systems of 1-inch diameter have resolution between 300-600 TV lines. With reference to memory, storage times from microseconds to minutes are obtainable.

A block diagram illustrating the use of a scan converter to provide a bright display of radar data together with map and computer video was previously shown in Figure 3-26. In Figure 3-38, a block diagram of the circuitry requirements for a single gun scan converter are shown. The mode switching for read, write, and erase is controlled by the programmer. In addition to static focusing, dynamic focus is also required to compensate for the variation of electron beam path length with deflection position. The protective circuits shown are required to cut off the electron beam in case of failure in the sweep circuits.

Dual-Gun Scan Converter Tubes

The double gun scan converters to be described have resolution varying from 600 to 1200 TV lines. Generally, the higher resolution is found in production tubes having a target diameter between 2 - 2.5 inches. Several of these tubes have been environmentally tested to full avionics environment. Further indicative of their suitability for an airborne environment are the following physical parameters-overall length: 16-1/2 - 20 inches; weight 7-1/2 - 9 ounces; diameter: 1-1/2 - 3 inches.

TUBE TYPE	MANUFACTURER	TAP	MAGN. FIELD	DEF. COILS	FOCUS	RESOLUTION TV LINES	MAX. ACCELERATION VOLTAGE	MTI	APPLICATIONS	
									SCAN CONVERTER	STORAGE
7225	WESTINGHOUSE		2.6	EL. STAT.	EL. STAT.	3100V	1000	X	X	
1E7-835	RAYTHEON		2	MAGN.	FL. STAT.	5000V	1200		X	
1E7-71	RAYTHEON		2	MAGN.	EL. STAT.	5000V	1200		X	X
KW-1	WARNECKE		2.5	EL. STAT.	EL. STAT.	1500V	1200	X	X	
6499	RCA		2.25	EL. STAT.	EL. STAT.	1500V	1000	X	X	
MTI-R	HUGHES		1	MAGN.	MAGN.			X		
WX-120	WESTINGHOUSE		1	MAGN.	MAGN.	1000V		X		X
WX-4291	WESTINGHOUSE		1	EL. STAT.	EL. STAT.	350V		X		X

Figure 3-37. Single-Gun Tubes

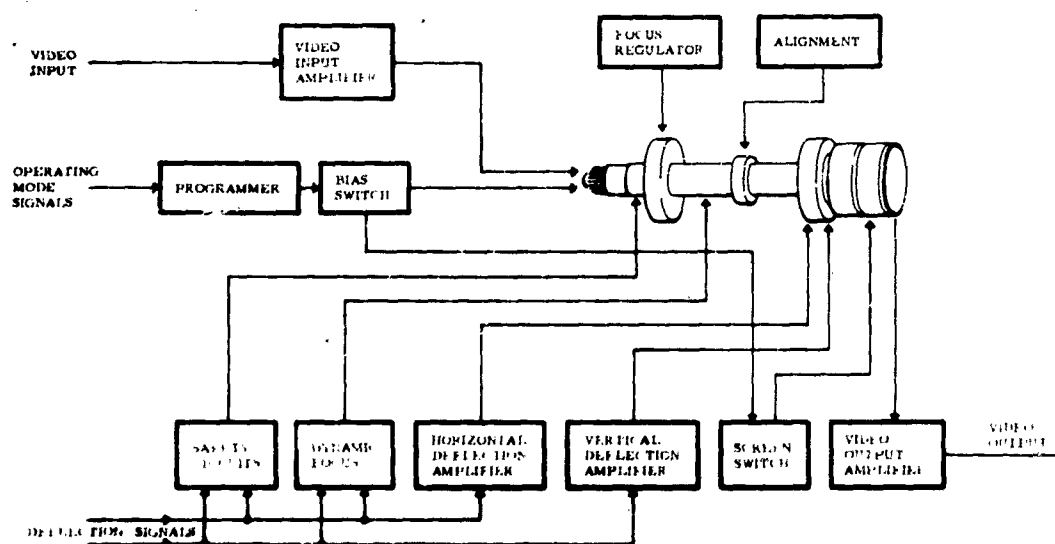


Figure 3-38. Single-Gun Tube Block Diagram

Double ended scan converters permit simultaneous writing and reading with sufficient persistence to preserve a full display of radar-sweep information, for example. From 7 - 15 shades of grey are reproduced. Some designs permit the input to be cut off and the last frame read for up to 30 minutes. An additional feature is the ability to selectively or totally erase stored information.

These features make double ended scan converters extremely useful for airborne applications.

1. EBIC

The EBIC dual gun structure is shown in Figure 3-39. This form of tube is manufactured by several manufacturers including Rauland Corp., Raytheon, RCA, and Warnecke. The principle components include:

- a. Writing gun and optics
- b. Reading gun and optics
- c. EBIC target

Writing Gun and Optics - The writing electron gun is either of tetrode or pentode design, producing a high velocity beam. The acceleration anode is operated at ground potential with the cathode at high negative potential (the filament transformer requires 10 KV insulation). Focusing is usually electrostatic while deflection is normally magnetic for high resolution. Note the absence of complex collimating lens systems. Electrostatic deflection has also been employed in special tubes to achieve recording speeds on the order of one-third the speed of light.

Reading Gun and Optics - The reading electron gun operates at medium beam velocities generated by accelerating voltages in the order of 1-2 KV. High resolution is obtained using magnetic focusing and deflection. Recent improvements to the read gun add an erasing electrode. This permits erasing the stored information sooner than the normal decay time.

Normal operation of the read gun, see Figure 3-40, is at 1-2 μA . To erase, the read electron beam is increased to 100 μA . This is accomplished by switching the erase electrode potential from anode potential

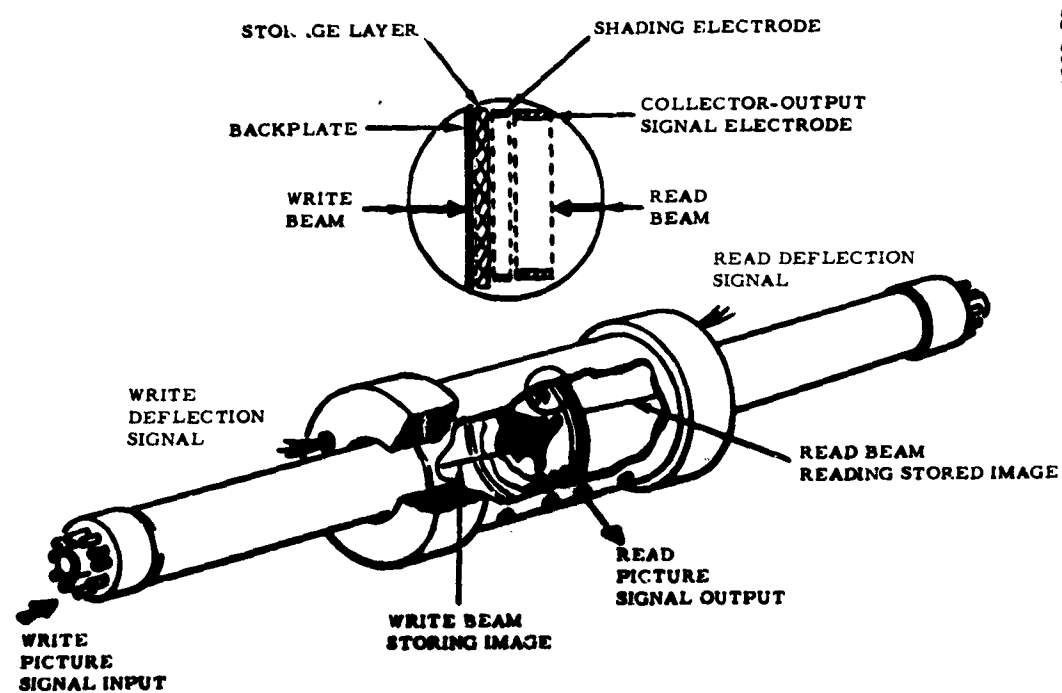


Figure 3-39. Dual-Gun Storage Tube (EBIC)

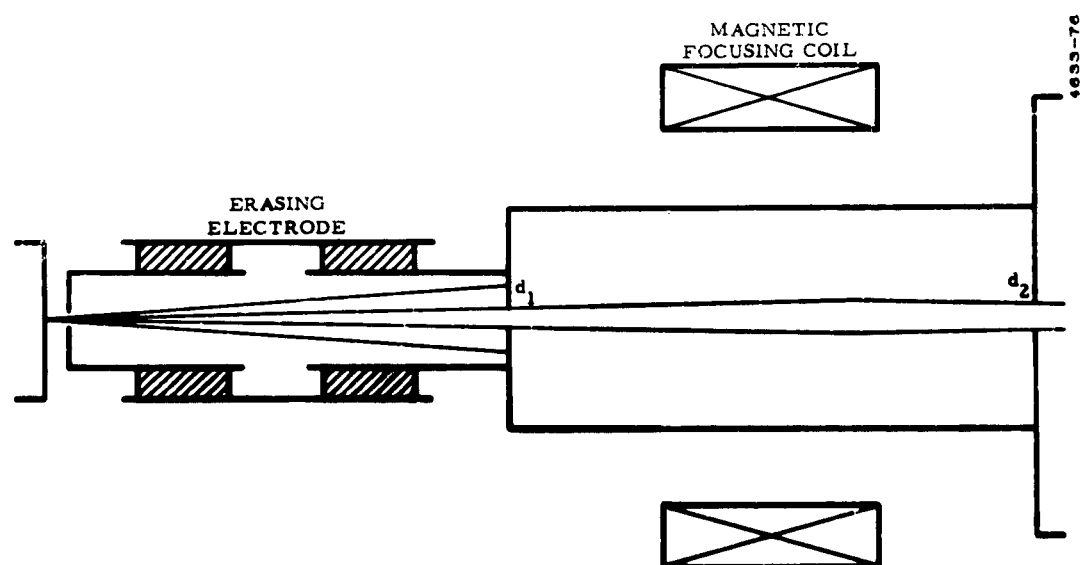


Figure 3-40. Normal Operation of Read Gun

(1 KV) to approximately -700 volts with respect to the cathode, see Figure 3-41. The read electron beam current impinging on the target, rapidly brings it to equilibrium potential. Good beam focusing is not required for the erase.

EBIC Target - The EBIC target is also shown in Figure 3-39. A thin metal backplate faces the write gun. On the read side of the backplate is a placed storage layer of either a dielectric or more recently, a doped semiconductor material. Also on the read side, a cylindrical shading electrode is included. This acts to insure uniform collection of the secondaries from the entire target insulating surface. Otherwise the secondary beam will have a signal synchronous with the scanning pattern. The secondaries are collected by the cylindrical collector shown in the figure.

Operation - In the dual gun tube, the write and read guns operate independently and simultaneously. The unmodulated read gun beam in effect tends to charge the elemental capacitors which comprise the EBIC target in a positive direction. This is accomplished by operation of the read gun at potentials such that $K > 1$. The high energy write beam, modulated by the signal, penetrates the thin backplate and discharges the storage target at each point in proportion to the instantaneous beam modulation. By adjusting the backplate to collector potential and the reading gun beam energy, the desired display persistence is obtained.

The action of the high energy write beam in discharging the target is as follows. The beam penetrates the thin backplates and produces ions along its path in proportion to the instantaneous modulation. The localized high resistance of the storage is thereby altered and a conductivity is induced. The resultant induced current reduces this point of the storage layer to a less positive potential, i. e. discharges the elemental capacitor in proportion to the beam modulation. As the read beam scans this point of the target, a different secondary emission ratio is induced, resulting in a video output signal proportional to the modulation. The significance of the acronym EBIC (electron beam induced conductivity) should now be apparent.

One problem with the EBIC is the possibility of induced cross talk caused by simultaneous scan of the target by the read and write beam. In earlier EBIC scan converter systems, this problem was obviated by

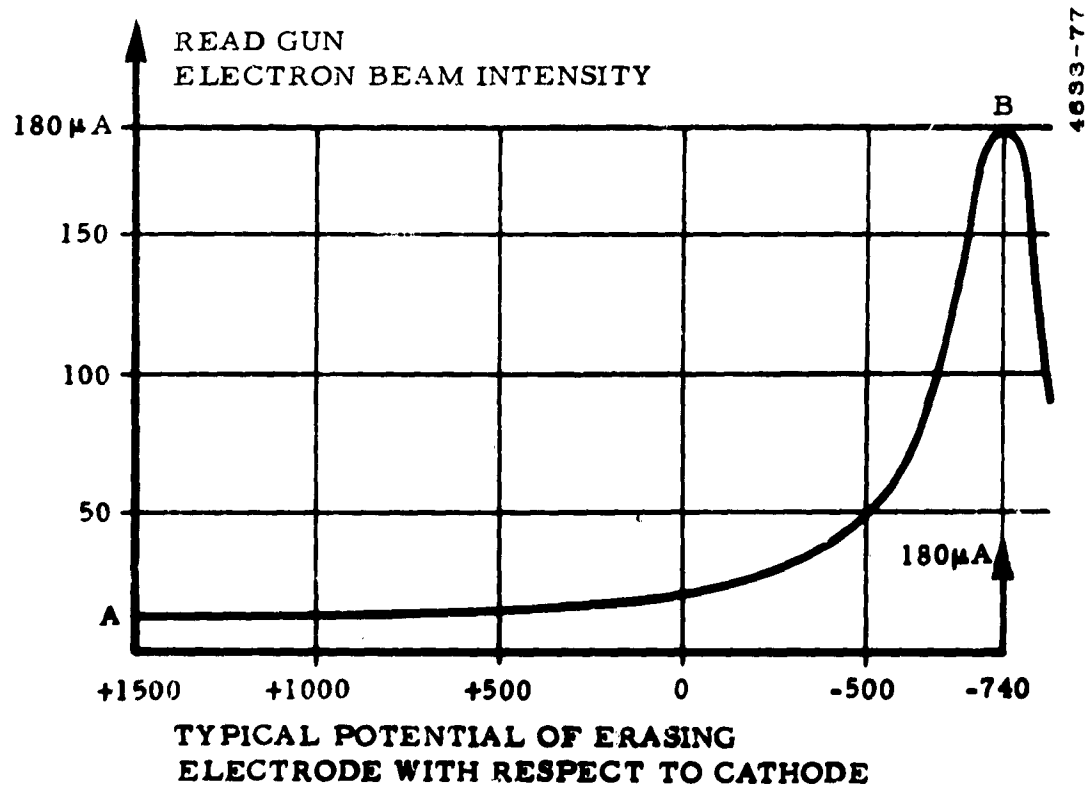


Figure 3-41. Read Beam Current with Erase Electrode

incorporating various video cancellation techniques. Recent EBIC tubes have eliminated cross talk as a problem. This has been accomplished through new target materials and increased target thickness.

2. Transmission Grid Modulation Tube (TGM)

In the TGM dual-gun scan converter, the write and read guns are identical and the target is centered between them, see Figure 3-42. This contrasts to the EBIC case where write and read guns are basically of different design. Another point of difference is the target structure and method of avoidance of cross talk. These will now be discussed.

a. Write and Read Guns and Optics

Both guns employ a high resolution tetrode design. The acceleration potential used is 5-6 kv. Electrostatic focus is used to obtain uniform spot size across the entire storage screen area through dynamic correction to the focus as a function of scanning angle. Where this is not a consideration, magnetic focus is customarily used. Deflection is magnetic. Both guns also employ collimating lenses L_1 and L_2 to provide a beam orthogonal to the target.

b. Target

The target is comprised of four screens having mesh density of 500-1000 lines/inch. Starting on the write gun side, the screens are as follows: 1) write decelerator; 2) collector; 3) storage screen; 4) read decelerator. The storage screen is coated on the write gun side with a dielectric. It is similar to the target described for the single gun RST.

c. Operation

The writing beam modulated with the input video signal scans the target, causing secondary emissions. Thus, the storage loses electron charge in accord with the video information. The unmodulated scanning read electron beam is allowed to pass through to the collector at an energy level proportional to the stored video pattern. Where no information has been written, the negative charged storage area completely cuts

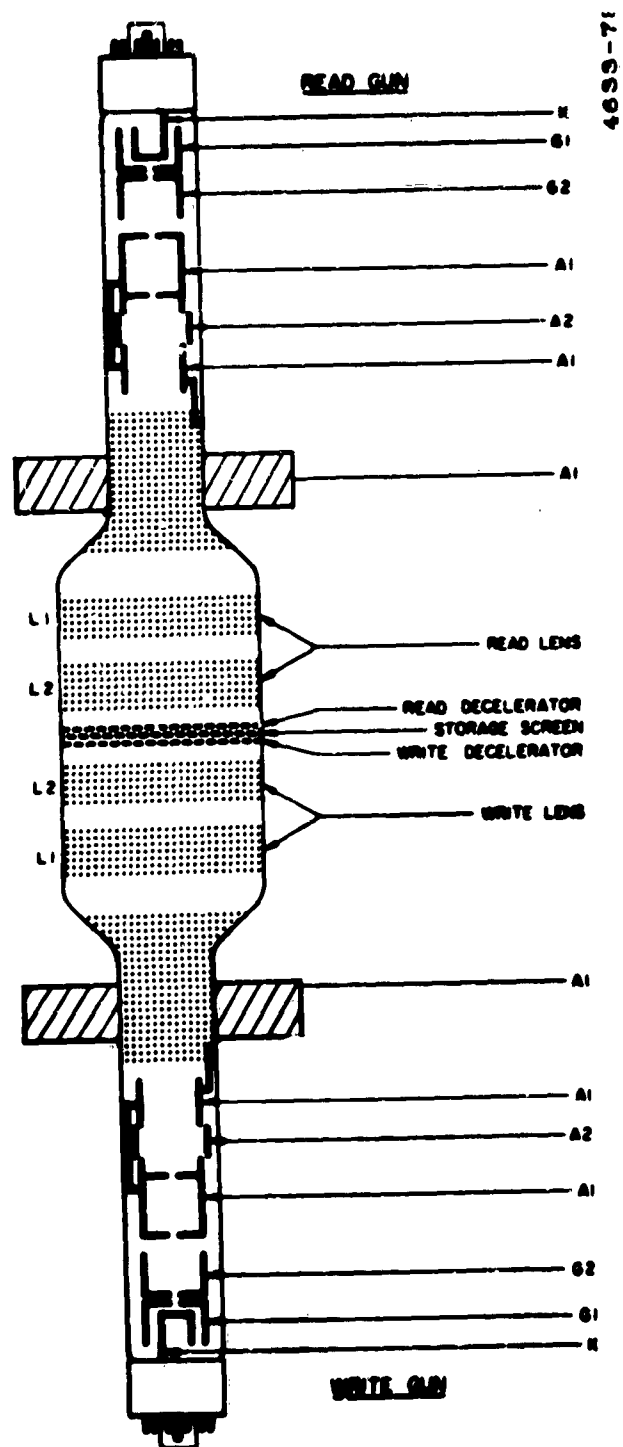


Figure 3-42. Schematic Drawing -- CK-7572/QK-703-TGM

off the read beam, thus establishing the "black" level. Correspondingly, fully charged positive points establish the "white" level. Levels of charge between these extremes correspond to the grey shades.

To avoid cross talk due to both write and read beams striking the collector simultaneously, RF modulation is used. Usually this is accomplished by modulating the read beam with a 30 - 60 mc/s carrier signal. The output is passed through a high frequency bandpass filter, thereby eliminating the low frequency write beam perturbations.

3. Fiber Optics Photon Transfer (FOPT)

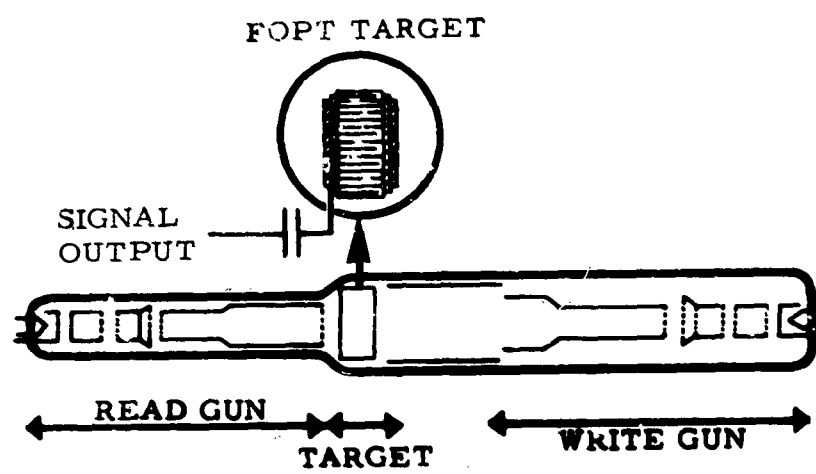
The FOPT is a double ended scan converter with a unique fiber optics coupling of the writing and reading sections. An important advantage derived is the elimination of cross talk problems. The FOPT dual gun and target structure are shown in Figure 3-43. The write gun and phosphor side of the target comprise a small CRT coupled by fiber optics to a vidicon pickup tube on the read side.

a. Write and Read Guns and Optics

The write and read guns are conventional high resolution types. The write gun is operated at 5000 volts acceleration potential with the anode grounded. The read gun acceleration potential is 300 volts with the cathode at ground. Writing beam current is on the order of .02 microamperes. Focusing of the write beam is electrostatic, requiring 1 kv at the focus electrode, while magnetic focusing is used for the read beam. Write and read deflection are magnetic.

b. Target

A detail of the target structure is shown in Figure 3-44. The fiberoptics disc is coated on both sides with a transparent conductive lamina. A layer of P-20 phosphor is deposited on the transparent lamina facing the write gun and a photoconductor layer on the read side. The output signal is derived from the transparent conductive lamina on the read side.



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Figure 3-43. FOPT Scan Converter Tube

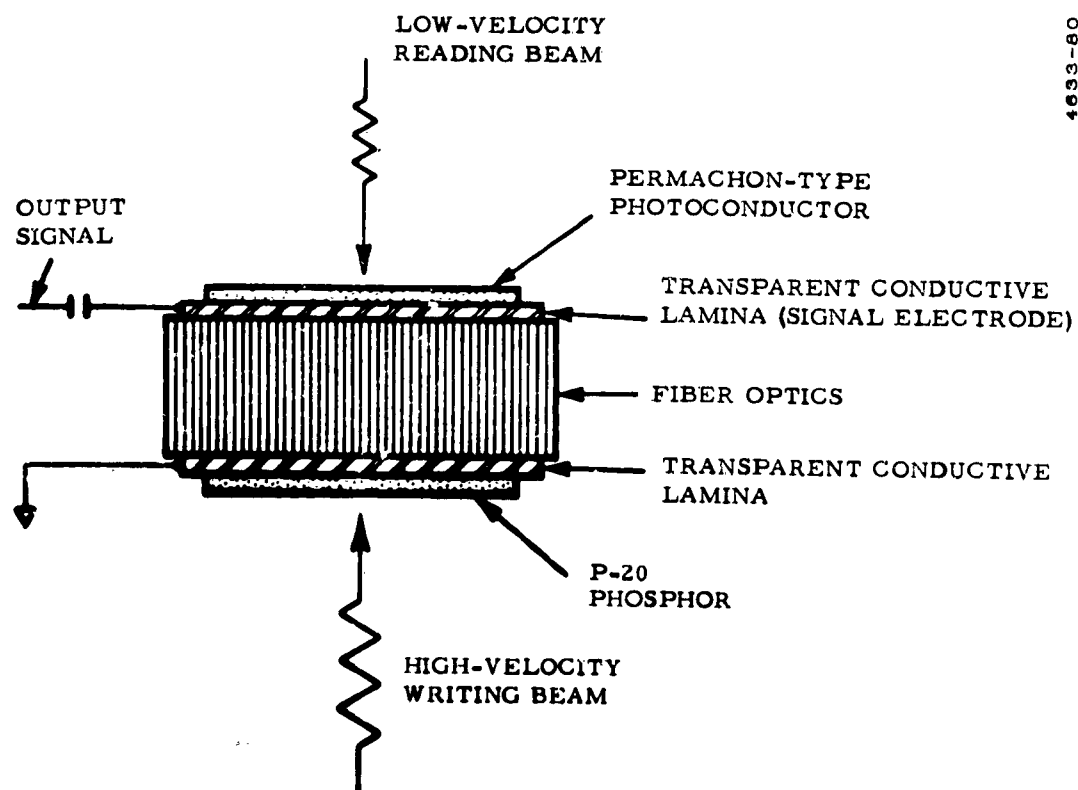


Figure 3-44. Fiber-Optics Target Structure

c. Operation

The operation cycle for FOPT type scan converters require three steps: (1) charge down; (2) writing; (3) reading. As in other dual-ended scan converters, simultaneous writing and reading is permitted. In addition, a frame of information, once written, may be stored for up to 30 minutes and read out at standard TV frame rates.

(1) Charge Down

Charge down is required prior to writing new information. This consists of applying 5-20 volts to the signal electrode (transparent conductive lamina on read gun side) and scanning the target with the reading beam. Electrons are deposited on the photoconductor until its potential is at the same level of the read gun cathode. Charge down requires 100 milliseconds or approximately 6 TV fields.

(2) Writing

The modulated write beam scans the target, producing a visual image of the information on the phosphor. Photons, emitted by the phosphor, pass through the fiber optics coupler to the photoconductor.

For a given level of signal output, the higher the writing beam current, the higher the writing speed permitted, see Figure 3-45. However, an upper limit on the order of .050 microamperes is set by consideration of the read beam inability to maintain the potential gradient across the photoconductor at higher currents (i. e. lower target resistivities).

(3) Reading

The photoconductor (PC) target areas, which are illuminated during writing via photon transfer, increase in conductivity. As a result, electrons which were deposited during charge down flow from the PC to the signal electrode which is at a positive potential. The illuminated areas of the PC thereby rise in potential and therefore acquire electrons from the unmodulated scanning beam. This produces the output video signal.

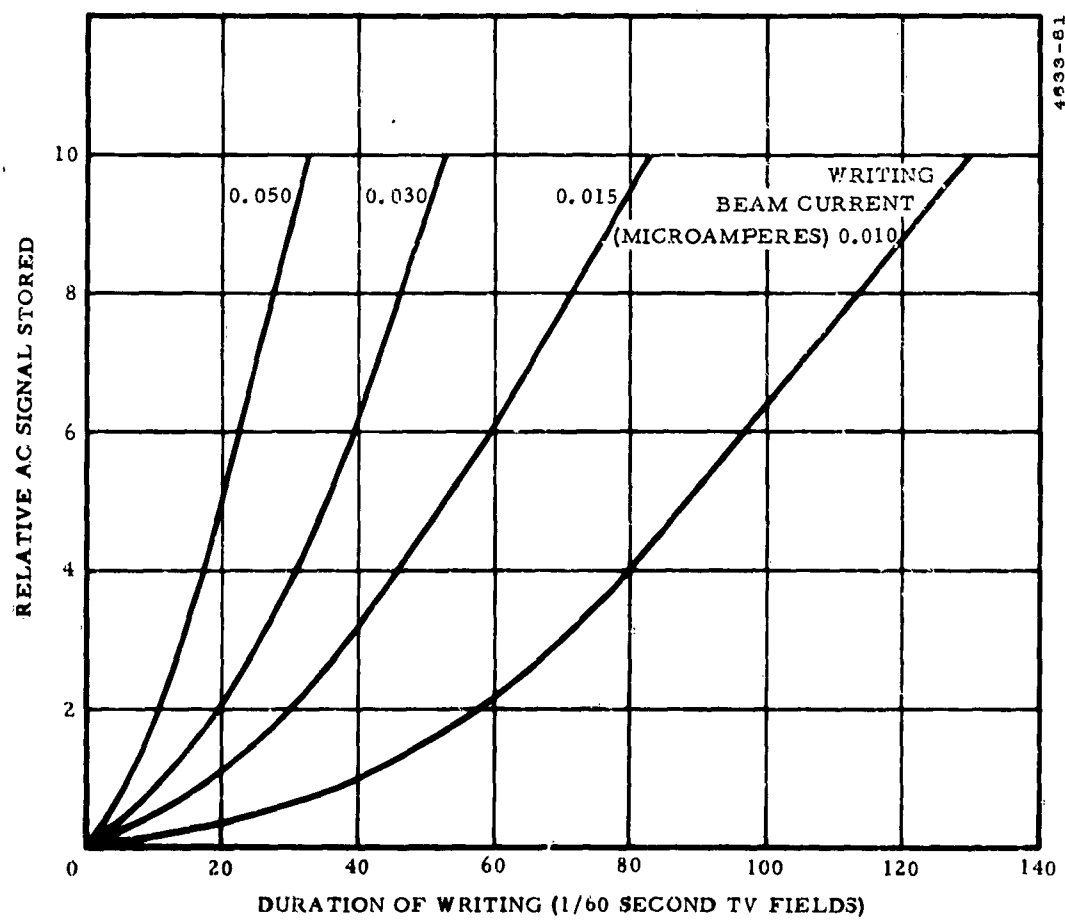


Figure 3-45. Writing Characteristic

(4) Erasing

Both enhanced and unenhanced erasure are available. Selective erasing is possible in either mode. Enhanced erasing requires 100 milliseconds or 6 TV frames. It is accomplished by flashing the phosphor target by the unmodulated write gun beam at illumination levels higher than required for writing. Enhanced erasing is independent of read beam action. In unenhanced erasure, the read beam is turned off. Decay of the stored information is shown in Figure 3-46, for various target voltages, and is seen to be an order of magnitude slower than unenhanced erasure, Figure 3-47. Enhanced erasure requires 6 TV fields.

3.3.5 Application Data for Dual Gun Scan-Converters

Figure 3-48, from reference 5 shows the application data for current scan conversion tubes. Data not shown in the table are the resolution and storage time. With the exception of the FOPT, the scan converters listed have a resolution in the order of 1000 TV lines. The FOPT with its 1 inch limitation on target size has a limiting resolution of 600 TV lines. With respect to storage times, a range from milliseconds to minutes is available.

3.3.6 Summary and Conclusions

The theory, operation, and characteristics of single and dual gun scan converters has been reviewed. Scan conversion has been shown to have many benefits for avionics display systems. Their use in an avionics environment entails no unusual operational difficulty. From the wide variety of available tube types, avionics displays may be now developed for operational use. It is predicted that scan conversion will be a central characteristic of the next generation of avionics displays.

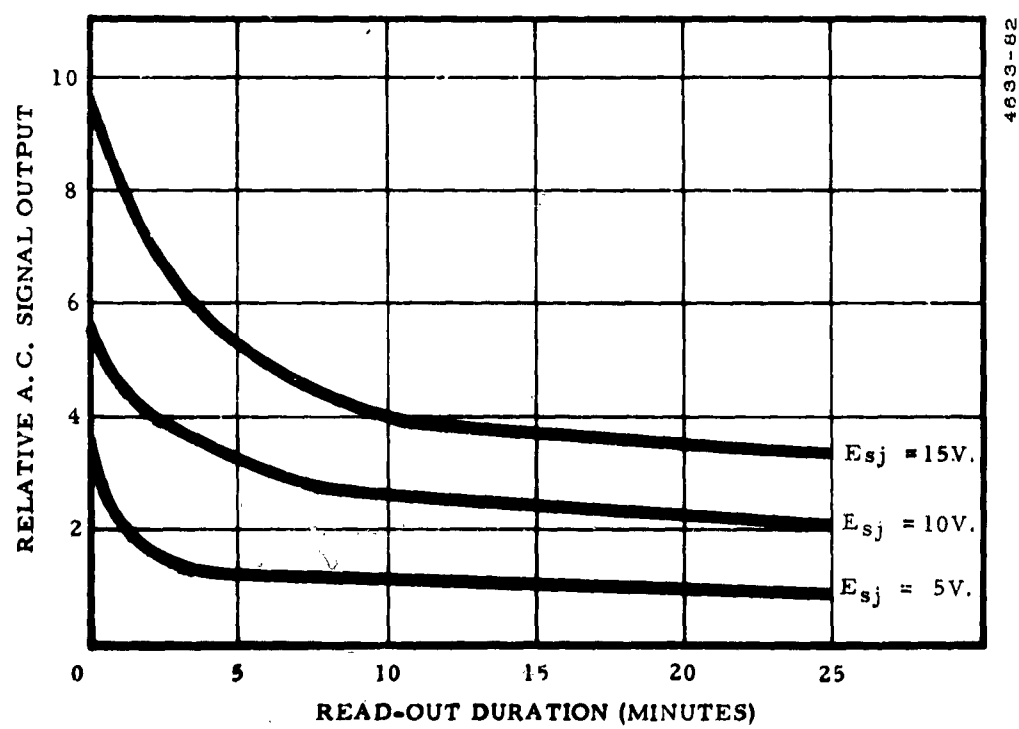


Figure 3-46. Storage Characteristic

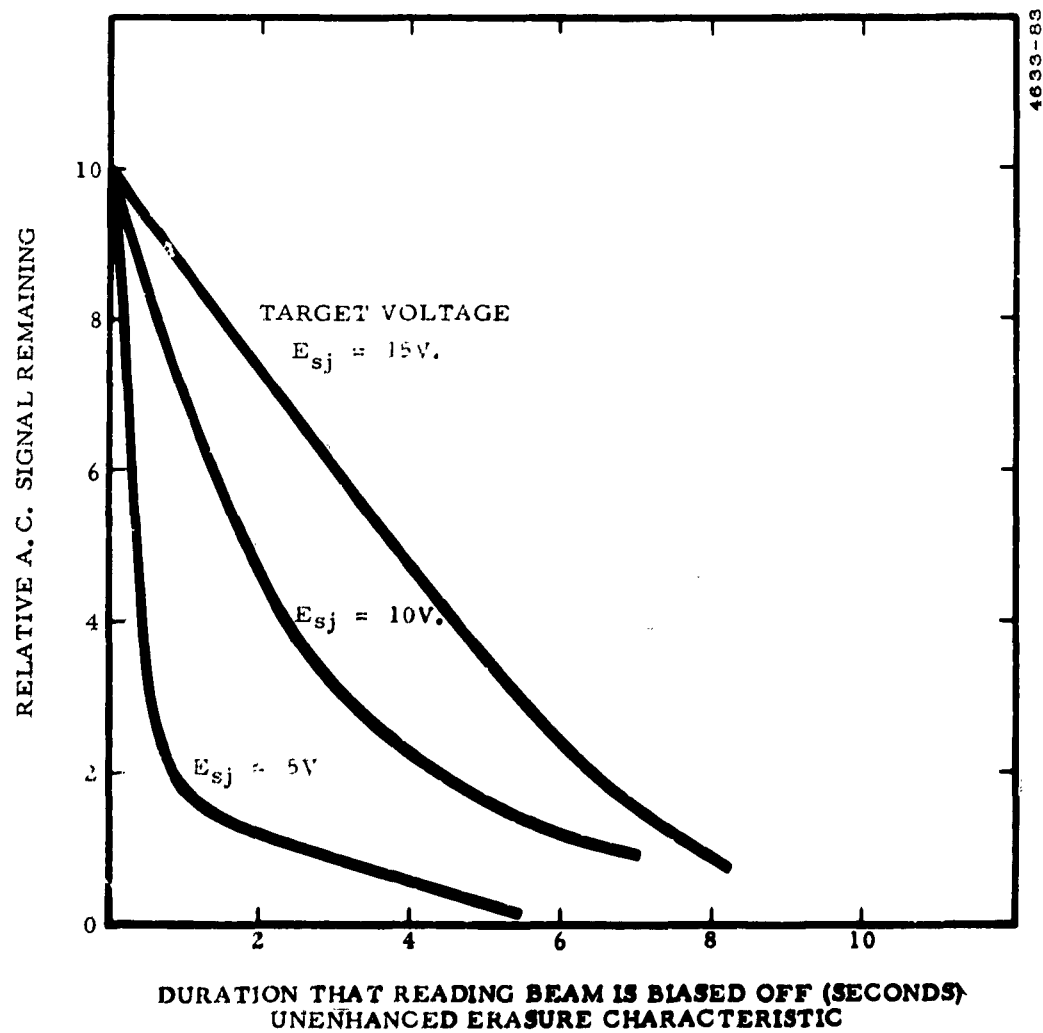


Figure 3-47. Unenhanced Erasure Characteristic

TUBE TYPE	MANUFACTURER	TARGET SYSTEM	TARGET DIAMETER INCH	DEFLECTION	WRITE SIDE			READ SIDE		
					FOCUS	MAX. ACCELERATION	DEFLECTION	FOCUS	MAX. ACCELERATION	DEFLECTION
CK1383	RAYTHEON	TRANS. MOD.	2	MAGN.	MAGN.	4.5	MAGN.	MAGN.	4.5	1.00
CK7792	RAYTHEON	TRANS. MOD.	2	MAGN.	EL. STAT.	3.5	MAGN.	MAGN.	3.5	12.00
7539	RCA	EBIC	2.25	MAGN.	EL. STAT.	10	MAGN.	MAGN.	2	12.00
R6215	RAULAND	EBIC	3	MAGN.	EL. STAT.	10	MAGN.	MAGN.	1.5	10.00
R6233	RAULAND	EBIC	3	MAGN.	EL. STAT.	10	MAGN.	MAGN.	1.25	10.00
R6253	RAULAND	EBIC	3	EL. STAT.	EL. STAT.	10	MAGN.	MAGN.	1.25	10.00
13038	RAULAND	EBIC	3	HELIX MAGN.	EL. STAT.	8	MAGN.	MAGN.	1.25	10.00
7508	GEL	EBIC	2.5	MAGN.	EL. STAT.	7.7	MAGN.	MAGN.	1.5	10.00
RW-5	WARNECKE	EBIC	1	MAGN.	EL. STAT.	6	MAGN.	MAGN.	1.5	8.00
RW-6	WARNECKE	EBIC	2.5	MAGN.	EL. STAT.	8	MAGN.	MAGN.	1.5	12.00
RW-7	WARNECKE	EBIC	2.5	MAGN.	EL. STAT.	8	MAGN.	MAGN.	1.2	12.00
WX-4640	WESTINGHOUSE	FOPT	1	MAGN.	EL. STAT.	5	MAGN.	EL. STAT.	0.5	6.00
WX-4821	WESTINGHOUSE	FOPT	1	EL. STAT.	EL. STAT.		EL. STAT.	EL. STAT.		6.00
174413	RCA	EBIC	2.25	MAGN.	EL. STAT.	11	EL. STAT.	EL. STAT.	2.75	
F3209	I. T. T.	TRANS. MOD.	2	MAGN.	EL. STAT.	3.6	EL. STAT.	EL. STAT.	3.2	1.00

Figure 3-48. Dual-Gun Tubes

3. 3. 7 Bibliography for Subsection 3. 3 Only

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2. Hergenrother, R. C., and Gardner, B. C., "The Recording Storage Tube", Proceedings of the IRE, July 1950.
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4. Doyle, R. J., "Permachon Type Scan-Converters", IEEE International Convention Record, 1963.
5. Nagy, G. T., "Scan Converter Tubes and Their Application", Information Display, March, April 1965.

3.4 COLOR DISPLAYS

The small-screen display of information in color is being approached through several techniques. The current number of TV programs in color and the public demand for color sets has created an incentive within research and development groups to accelerate the development of new color-display techniques. With all this push for color, definite published information on "shelf item" systems is sparse, but the state of art is advancing.

In a study of small-screen color display, such factors as method of obtaining display, number of colors displayed, system resolution, image repetition rate, image brightness range, and system complexity are of paramount interest and will require consideration. The methods of obtaining the display may be divided into four categories: (1) evacuated, (2) solid-state, (3) liquid, and (4) gas.

Advances in solid-state physics and improved methods in such fields as microminiature circuits, photo engraving, and precision mechanical manipulation have given impetus to research and development of new types of displays. The size of these displays may vary from 1 inch by 1 inch up to 5 feet by 5 feet and even larger.

Of the evacuated displays the cathode ray tube type is by far the most widely used at this time, and will remain so indefinitely in the foreseeable future, barring a major breakthrough in an entirely new display technique. Military application has been limited, however, due to the following factors: Inadequate color purity and saturation for good differentiation of hues; poor resolution; sensitivity to stray magnetic fields; and inadequate light output. Additionally, the mechanical drawbacks of the tube's sensitivity to shock, vibration, and stray magnetic fields, requirement for precise adjustment have also limited their use to commercial television. As indicated below, some of these limitations have been overcome.

Various other techniques have been suggested and sometimes used to achieve a color display. These include film systems, the use of multiple monochromatic CRT's with color filters, and the use of a monochromatic CRT with a rotating color wheel (the CBS TB system). These techniques are applications to achieve color and are not described here.

Since the first attempts to obtain color from a cathode ray tube, there have been numerous techniques proposed. All are of two basic

types: (1) a separate electron gun is used to energize each phosphor, with modulation of the electron beam(s) to determine the desired hue. Or, (2) one gun is utilized to energize all phosphors, with the color selection being by deflection of the beam. In the latter, the beam may be used to scan all phosphors and gated to determine the desired hue, or the beam may be discretely deflected to select the desired hue. A variation of this last method is to control the size of the beam bundle, so as to energize a different area of phosphor (as used for the Hughes Storage Color Tube).

All the suggested techniques will not be covered here; those excepted will be either because they never were realized in a working model or are variations of a more important technique. However, some techniques will be described that will undoubtedly never be used in operational equipment. Those then that will be described are:

Shadow Mask Tube

Lawrance "Chromatron"

Geer "Flat" Tube

Mullard "Banana"

Penetration Control

Goodman Radiation Indexing Tube

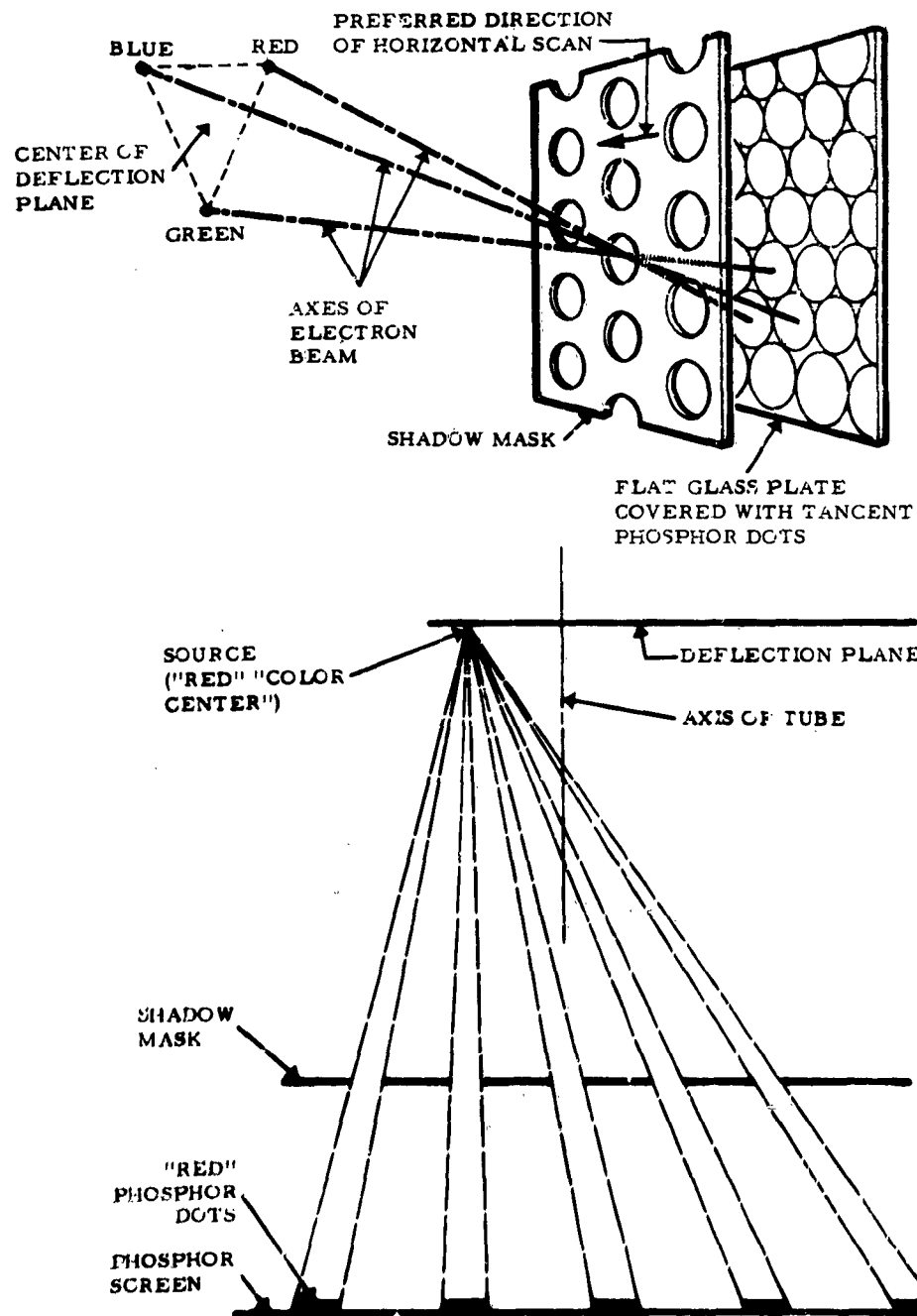
Hughes Color Storage Tube

EPIC (Electronic-Photochromic Integrating CRT)

Other methods, including Eidophor type, thermoplastics, and the use of the electro-optic effect in crystals will also be briefly discussed.

3.4.1 Shadow Mask Tube

The Shadow Mask Tube is representative of the color CRT technique which uses an electron gun for each phosphor. The construction of this tube is shown in Figure 3-49. The shadow mask, a thin perforated electrode, is placed close to the screen and registered with it, such that each hole in the mask coincides with a triad of three phosphor dots, one for each primary color. The gun alignment is such that only those phosphor dots of one type can be energized by each electron beam; by modulating the correct gun (or guns), the desired hue can be achieved.



4833-85

Figure 3-49. Shadow Mask Technique

Various other techniques have been suggested to achieve this direction of the electron beam. These include the use of complex surfaces, such as illustrated in Figure 3-50. The shadow mask technique has definite advantages over other methods, since only moderate angular separation between the electron beams is required; wide angular separation generally results in poor registration of the respective rasters.

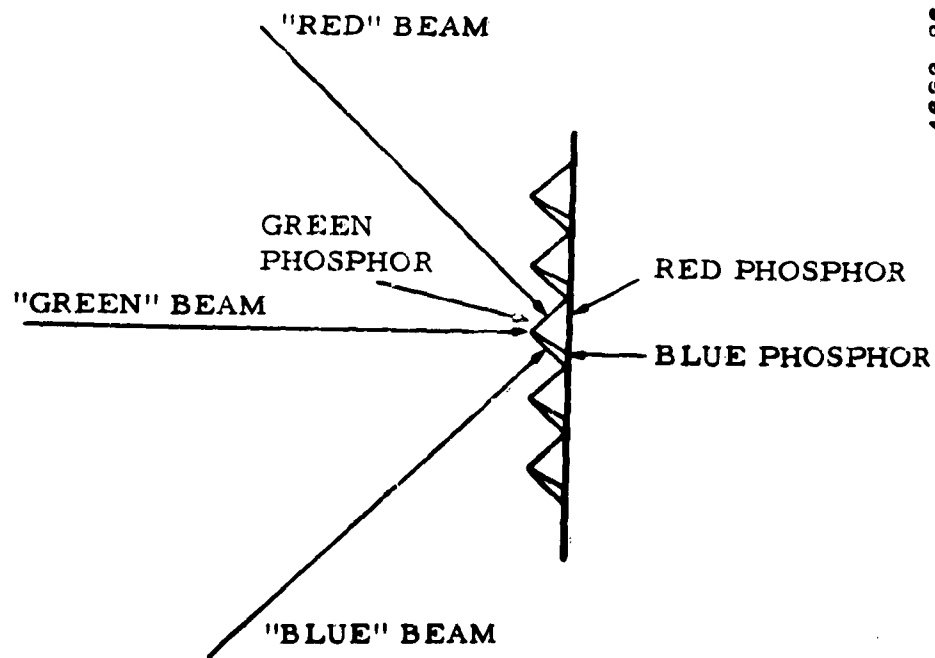
The shadow mask principle has also been used in a single gun color tube. Rather than have three guns, the approach of the electron beam to the shadow mask is controlled with a color-selection magnetic field.

Although shadow mask tubes have been found to yield satisfactory color pictures for commercial television, they do possess one serious drawback. Only approximately 15% of the total beam current reaches the phosphor screen, resulting in low light output. The tube is quite sensitive to stray magnetic fields, and so equipment associated with the CRT must be periodically degaussed. However, regardless of any drawbacks it may have, the shadow mask tube is the only color CRT in use in existing equipment.

The three-color shadow-mask CRT is currently available from several manufacturers in both circular and rectangular shapes. Color monitors are beginning to appear on the market. For example, CONRAC have color monitors designed for both broadcast studio requirements as well as industrial closed circuit system use. The broadcast monitor comes cabinet mounted, 21" tube while the industrial units are available in 17" rack version or as a 21" inch cabinet model. These monitor systems have the conventional television 525 line resolution. A high resolution shadow mask tube has been developed by RCA having one thousand line resolution in both viewing dimensions.

3.4.2 Lawrence "Chromatron"

The originally developed Chromatron tube, Figure 3-51 was a single gun, three-color device, using a fine, highly transmissive grid of horizontal wires placed close to the phosphor screen to effect color selection. The phosphor screen was comprised of thin parallel strips of alternate colors (red, green, and blue) with a pair of grid wires for each set of primary colors. With the grid uniformly charged, an electron beam passing through the grid is not deflected and energizes the center phosphor strip; by charging one wire positive to the other, the beam can be



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Figure 3-50. Complex-Surface Screen

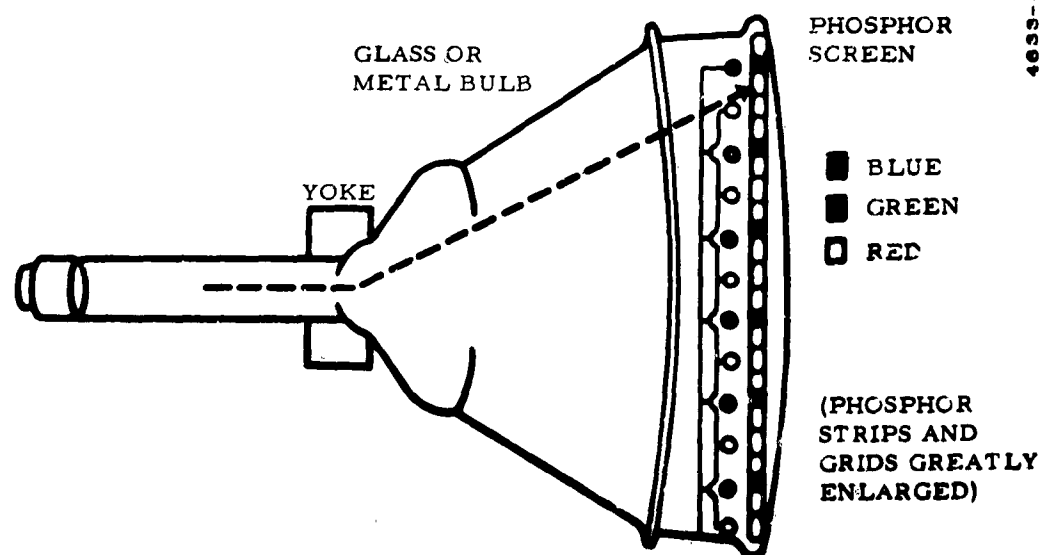


Figure 3-51. Chromatron Tube

deflected and a second phosphor is energized. By reversing the charge, the third phosphor can be energized.

Television systems utilizing the Chromatron were demonstrated as long ago as 1957; since that time, however, little improvement has been made to the basic system. Since a wire grid pair was required for each set of phosphors, the mechanical construction of the grid limited the achievable resolution. Additionally, the wire grid, unsupported except at the sides of the tube, limited the maximum size of the tube; the large tubes produced were very sensitive to vibration. The sensitivity of the tube to stray magnetic fields also limited its usefulness.

Two color versions of the Chromatron were also developed, but never actually used in a system. Recent development of the tube by the Chromatic Division of Paramount Pictures has eliminated the color switching grid and uses three electron guns, retaining the color-strips phosphor screen. The three guns are oriented so as to converge on their respective phosphors, while the equivalent of the original color-switching grid is used for post deflection focusing.

The **Lawrence-type** tubes have been made in various sizes with phosphor screen areas from about 6-1/2" to 22" in diameter with phosphor arrays ranging from 80 to over 125 strips per inch. In addition to the above referenced manufacturer, this tube also is currently being manufactured by Sony in a 3-color 9" version for use in their color TV system being used aboard commercial airliners for entertainment presentation to individual passengers. They are so far behind in back orders at present, however, that they have no published information available. The tube is also manufactured by Litton under the registered trademark of **CHROMATRON** and is completely described in their brochure "The Chromatron". Both two-color and three-color Chromatrons are available.

Hughes Color Storage Tube

The Hughes Color Storage Tube is basically identical to the conventional direct-view halftone storage tube; the phosphor screen, however, is comprised of an array of phosphor dots corresponding to and aligned with the holes in the storage mask of the storage-target assembly. Each dot is surrounded by a field of a second color phosphor. Tube construction is illustrated in Figure 3-52a. Details of the storage tube screen are shown in Figure 3-52b.

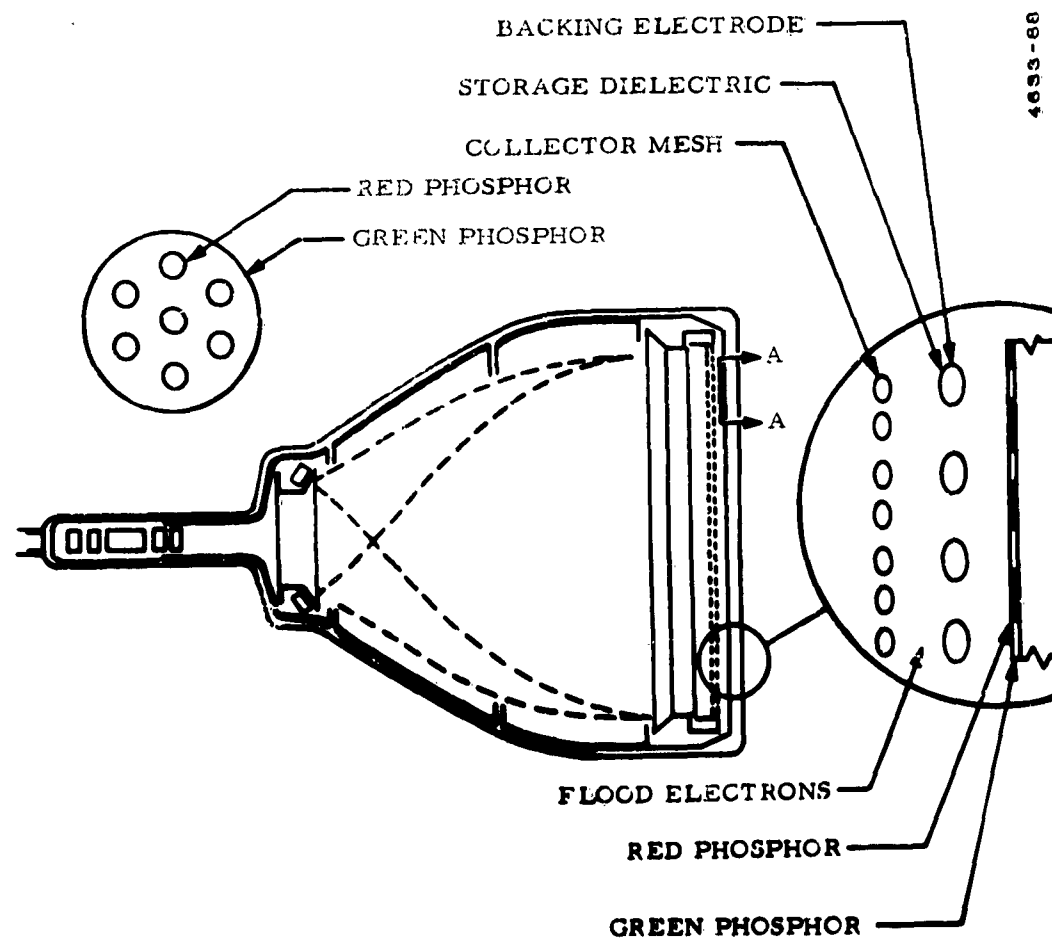


Figure 3-52a. Hughes Two-Color Storage Tube

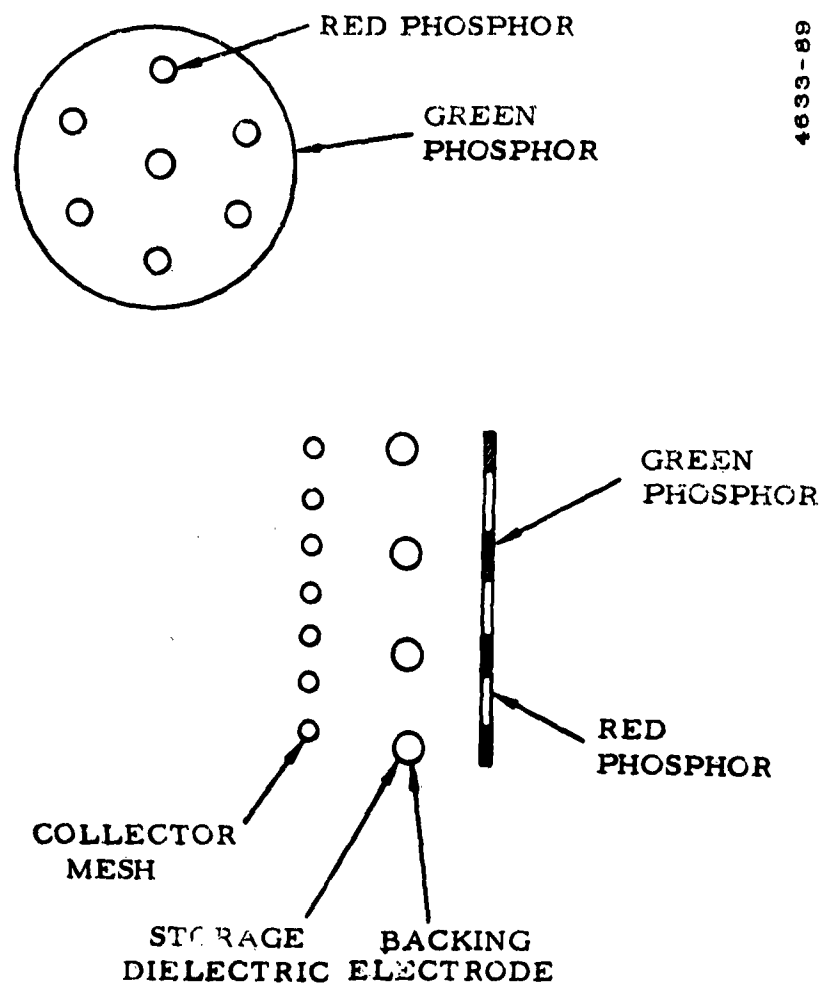


Figure 3-52b. Color-Storage Tube Screen Details

Flood electrons which pass through the storage mask holes, when the storage-surface potential is near cutoff, fall within small areas of the viewing screen, aligned with the holes in the storage mask. As a result, only the phosphor at the center of the "donut" is excited. If the storage-surface potential is near that of the flood-gun-cathode potential, the flood electrons are dispersed and fall on overlapping areas of the screen, exciting both the hole of the "donut" and the "donut" itself. By proper selection of the phosphors, two reasonably pure colors and the shades in between can be selected. Figure 3-52c indicates the overall transfer characteristics, using red-green phosphors.

The characteristics of the Color Storage tube, as stated by the manufacturer, are:

Physical Size	10-1/2" Diameter; 18" Length
Screen Size	7-1/2" Minimum Diameter
Deflection	Electromagnetic
Color Range	Red, orange, yellow, yellow-green
Resolution	50 to 60 lines/inch, 80 relative luminance
Luminance	30 to 90 Foot-lamberts
Persistence*	Approximately 15 minutes/volt of storage surface potential shift
Writing Speed	150,000 volt-inches/second
Operating Potentials	10 KV Viewing Screen -3.5 KV, Write Gun Cathode

3.4.3 Geer Two-Color Thin Tube

The Video Color Corporation of Inglewood, California has adapted the principles of the Kaiser-Aiken Thin Tube to a two-color thin tube. Figures 3-52d and 3-52e depict the Geer Color Thin Tube. The single gun as used in the Aiken tube has been replaced with two guns, mounted at one end of the glass "box", and the two color phosphors have been deposited on opposite sides of a thin glass screen. The screen is positioned such that one gun impinges on one side of the screen and the second gun impinges on the other side. The two guns and the deflection

*Controlled persistence (electronically controlled decay of stored information) is not possible on this tube without a shift of color as the information is erased.

SCANNING RATE 25,000 IN./SEC.

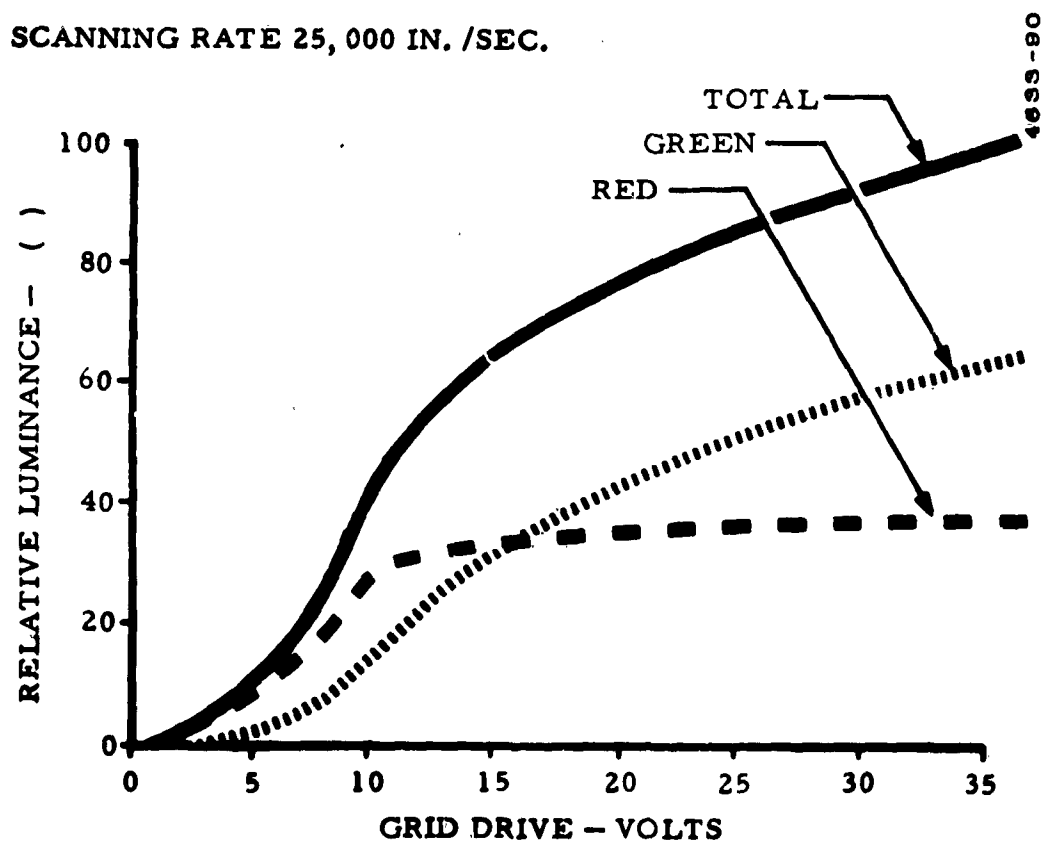


Figure 3-52c. Average Transfer Characteristics

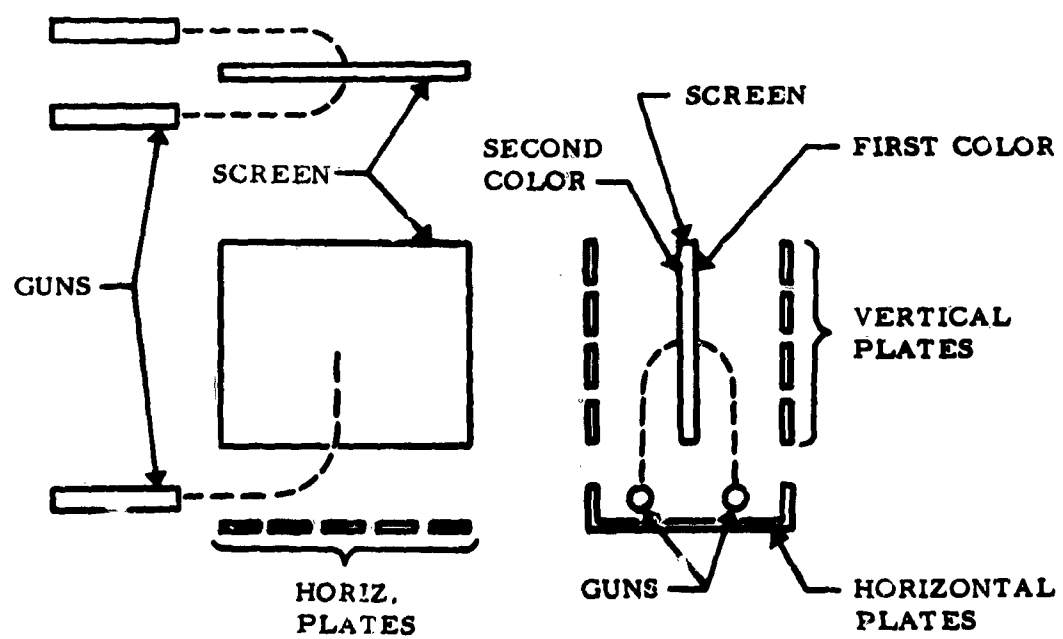
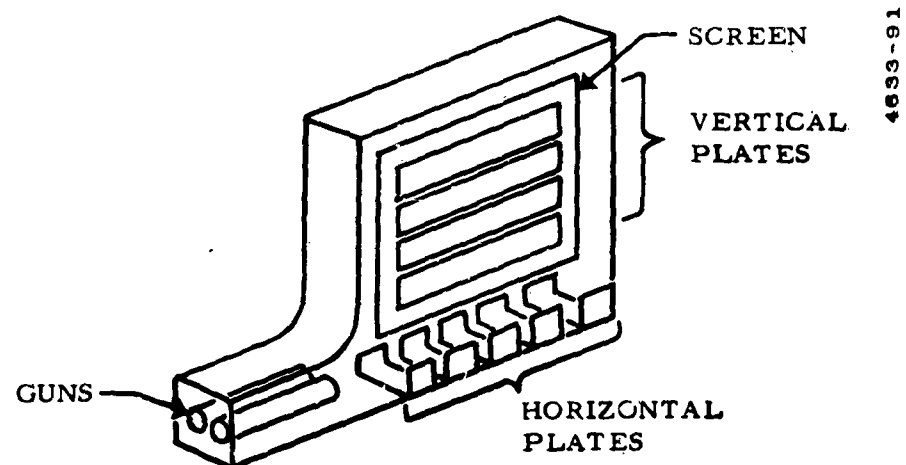


Figure 3-52d. Greer Two-Color Thin Tube

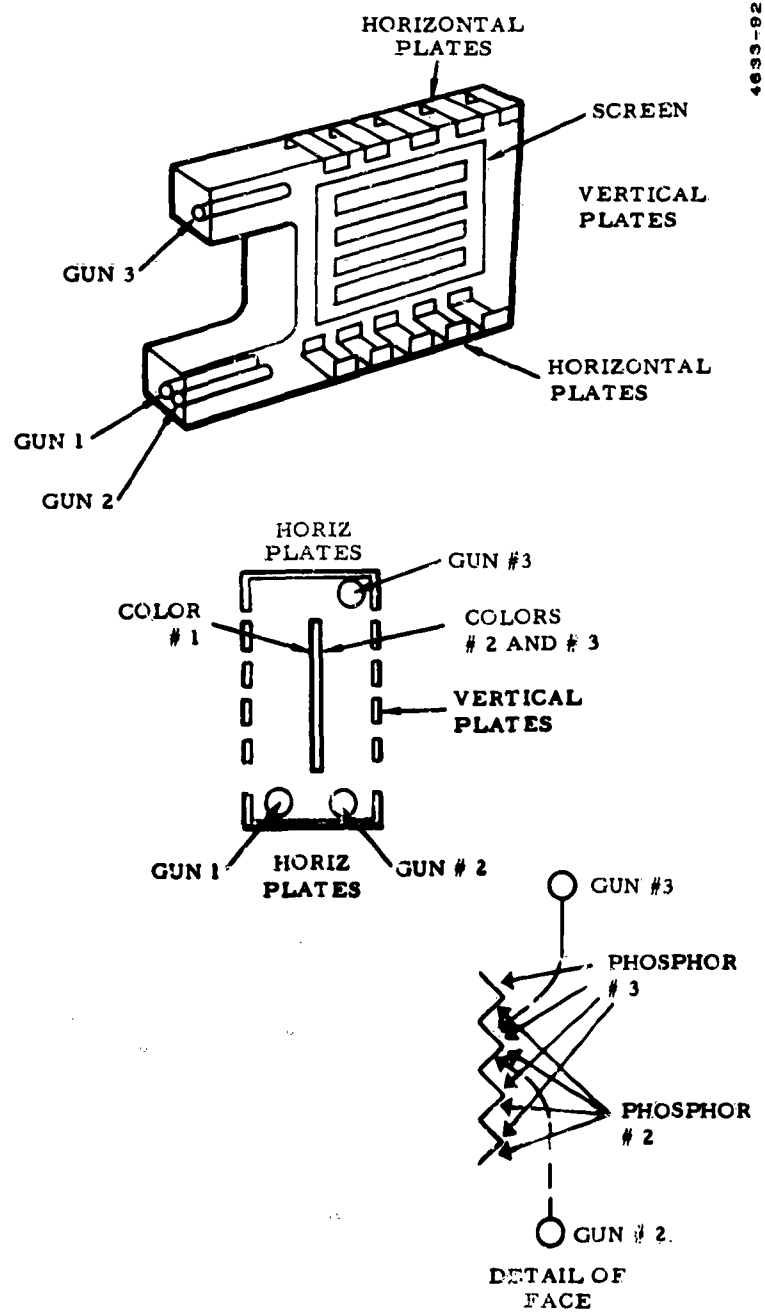


Figure 3-52e. Three-Color Thin Tube

system are synchronized, to achieve perfect color registration. Focusing is electrostatic which deflection is electrostatic in the vertical direction and electromagnetic in the horizontal direction.

This technique offers high resolution, high brightness, and is not subject to disturbance due to stray magnetic fields. There is a size limitation, due to the limitation of mechanical strength of the glass sides of the box; special techniques for increasing the strength of the glass are being investigated.

The Geer-Color Thin tube has been demonstrated, but is not in production; major company effort is being expended on monochromic thin-tube development. Since the experience gained with the monochromic tube should be directly applicable to the color version, it is safe to assume that the thin color tube will be perfected. Circuitry limitations will likely limit its use to systems employing television scan, however, due to the problems associated with addressing the individual deflection plates and the high voltages at which they are operated.

Other characteristics are as follows: The tube is essentially a rectangular parallel-piped with approximate overall dimensions of thickness 2-5/8 in., width 10 in. and height 8 in. (excluding gun protrusion). The overall height including the two-gun protrusion into the 10 in. slide is about 20 in. A wide variety of the two colors displayed and image persistence is available since the choice of the two phosphors is arbitrary. Presently about a 10-min spot size is being achieved, so that resolution is about 600 TV lines in the 6 in. x 8 in. field of view.

3.4.4 Mullard "Banana" Color Tube

The Mullard "Banana" tube is best characterized as a color line-scan tube. As shown in the illustration, Figure 3-53, three color phosphors are laid parallel to each other and in line with the electron gun. Electronically, the beam is made to scan from one end of the stripes to the other, all the while being wobbled so as to hit all three color phosphors. This has the effect of giving a single line scan, the color of which can be controlled by gating the electron beam at the appropriate time.

A vertical scan is accomplished external to the tube, by the use of rotating cylindrical lenses and a hyperbolic mirror.

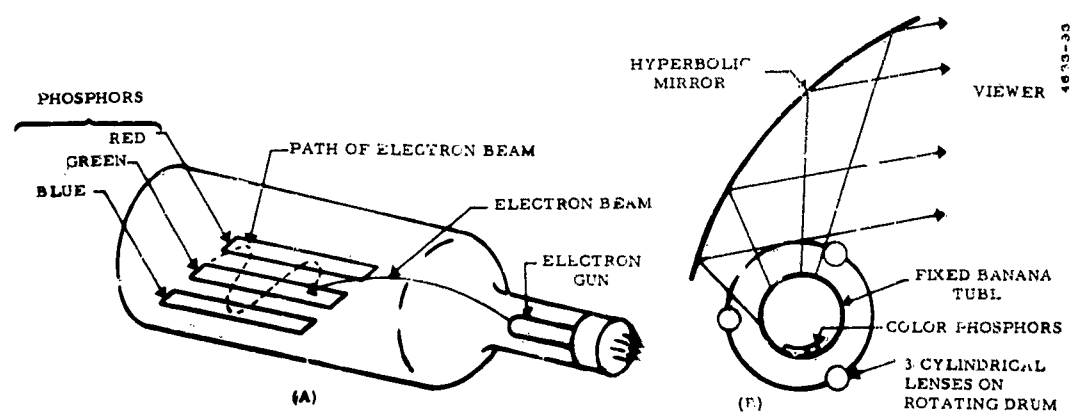


Figure 3-53. "Banana" Tube

A light output of forty foot-lamberts at a mean beam current of 400 microamps has been claimed for the tube. However, like virtually all line-scan tubes, the high power into the phosphor results in rapid deterioration of the phosphor efficiency. This, together with the mechanical problems involved with the rotating lens system (noise, wobble, wear), make the system impractical for a commercially producible unit or for military systems.

3.4.5 Penetration-Control Color Tube

Controlling the penetration of a series of phosphor layers to produce different colors has been used in several color tubes. Figure 3-54 illustrates the construction of such a tube. Either a single gun or three separate guns may be used. Typically, the difference between penetration of the layers is 4KV/layer. In the case of separate guns, the individual guns are biased at the required voltage relative to the anode. With the single gun unit, the anode voltage itself is switched. One of the drawbacks to the single gun system is the rate at which anode voltage can be switched to achieve the full range of hues; presently achieved rates are far short of that required for commercial television. However, with random display units, the switching can be programmed to take place while beam positioning is occurring.

One of the drawbacks to the development of penetration-control tubes has been the lack of high brightness, transparent, color phosphors. However, the process for making transparent phosphors has been improved, so this should not restrict the future development of this technique. Very high resolution has been claimed for the newer transparent phosphors, together with advantages due to the absence of reflected light from these.

Typical of this type of tube is the Penetron (General Electric Company) and the Transylume (Panaura Corporation).

3.4.6 Goodman Radiation Indexing Color Tube

The Goodman Radiation Indexing Color Tube depends upon the emission of radiation as a scanned electron beam strikes a wire index*, using this

*The use of an indexing strip to sense the exact position of the beam was also used in the Philco "Apple" tube of 1957. Here the index was a phosphor, deposited to the rear of the aluminized layer, and was detected and used to retain registration.

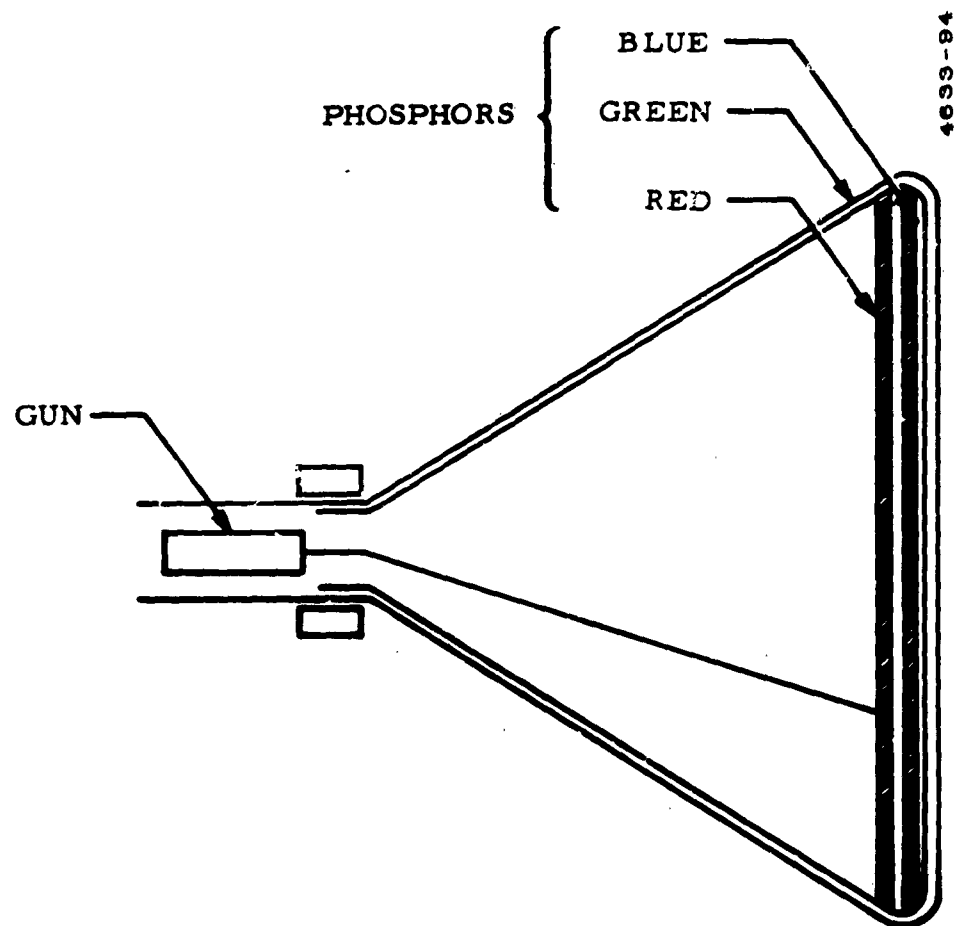


Figure 3-54. Penetration Control Tube

detected radiation to synchronize the color demodulation system. This tube uses a single conventional gun and a color screen comprised of vertical red, green, and blue strips, with an indexing strip (or wire) between each group of three color strips (see Figure 3-55). As the electron beam is scanned across the color groups and hits the index wire, X-Rays are generated. These are detected by a scintillator coating on the end of a light pipe, and the light is transmitted through the light pipe, detected, and used to produce an indexing pulse. Utilizing this indexing pulse, the modulation of the electron beam is controlled to ensure registry of the beam on the proper phosphor.

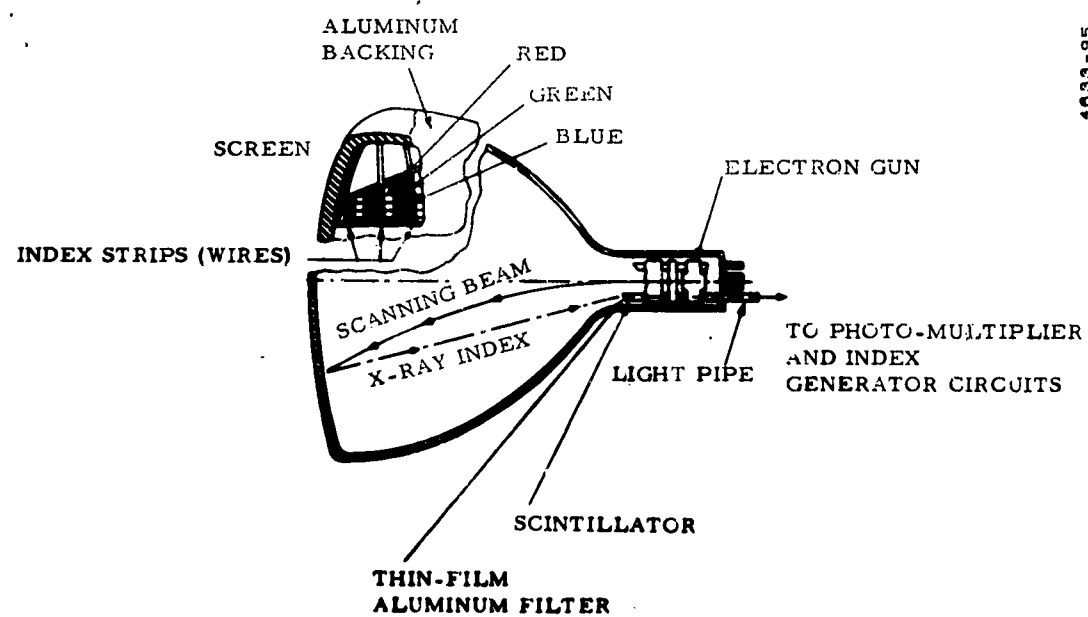
A suggested modification of the Goodman Tube utilizes a special (P16) phosphor strip instead of wire indexing strips, and the ultraviolet emitted is passed through the light pipe and detected. In this modification, no scintillator is required.

The Goodman Tube is still in the development stage, and, although several CRT manufacturers have expressed interest and a patent has been granted, it cannot reasonably be considered for system useage within the next few years. Plans call for production of a 600 line, 75 ft. lambert, 21 in. round and 23 in. rectangular tubes.

The basic design limits its useage to a "scan" mode of operation, since a reversal of direction of scan would result in erroneous synchronization. The basic simplicity of the tube should make it cheap to produce and result in higher resistance to shock and vibration than most other color tubes. In addition, the only limit to size should be purely mechanical constraints; bulb strength and weight.

3.4.7 Other Methods

There are several other methods that should be mentioned in a discussion of small screen color display, even though they are more in the nature of large screen systems, and in general require large bulky equipment. The Eidophor system is a light modulating method employing a CRT type electron gun that creates an electrostatic pattern in an oil film. This in turn acts as the image in a complex Schlieren projection system. Color is achieved by an additive process whereby a rotating optical filter sector wheel introduces a red, green, and blue filter consecutively into the projected beam at a frequency high enough above the persistence of vision but synchronized with field repetition rate such that the eye integrates the colors without the sensation of flicker.



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Figure 3-55. Goodman Radiation Indexing Color Tube

The General Electric Company has developed two systems similar to the Eidophor. They are referred to as the Talaria Color Light Valve System and the Sealed Tube System. These systems differ from the basic Eidophor in that the projection is through the surface with the oil film deposited on it rather than being reflected from a nearer surface. The Sealed Tube System was developed under contract from U.S. Navy Bureau of Ships, and has been successfully demonstrated at the Naval Electronics Laboratory, San Diego.

G. E. has also developed another system that uses a film with a thermoplastic coating that accepts electrons from an electron gun to form an electrostatic picture image, developed by heat, and Schlieren projected. This system was described in an article by W. E. Glenn, "A New Color Projection System" in the November 1958 issue of the Journal of the Optical Society of America. Also a 16mm portable thermoplastic recorder is described in an article by the same author, "Thermoplastic Recording: Progress Report" in the Journal of the SMPTE, August 1965. Further information is given in a G. E. brochure "Thermoplastic Picture Recording". Quoting from this brochure on color, they say, "One of the most important characteristic of thermoplastic recording is its capability for low cost recording and projection in full color pictures. All color information is written simultaneously on each frame with one electron gun. Similarly, the color projection system requires a single set of optics.

Solid state display systems are presently in an experimental phase with very meager definite information available. An article in the Journal of the Society for Information Display, March/April 1965 by Edward J. Calucci, describes the experimental work at Rome Air Development Center on a solid state light valve based on the electro-optic effect. The work so far is for a monochrome system with the idea of developing a system to include full color capability later. The system employs light projection of a light source, such as a xenon arc, collimating lens, optical polarizer, electron gun modulated electro-optic effect crystal, a polarization analyzer, a projection lens and finally a projection screen. This system, as described, produces black and white displays only. Method of producing color was not pointed out, but it is possible that some of the known additive techniques might be applied here also.

3.4.8 Conclusion

Of the presently available methods of small screen display in color, probably the first choice should be the shadow mask CRT as developed by RCA. This choice is based on its wide use in the current commercial television expansion into color display. This type CRT is being manufactured in quantities by many companies in various sizes. Public demand for color TV has accelerated its perfection. It is immediately available for system application as a reliable component.

As a second choice the Aiken thin-type CRT, two color or three color appears to have a slight edge on the Chromatron. It is somewhat more simple to manufacture and has a greater resolutions potential than the Chromatron. Neither tube has been widely used so far, so that reliability has not been established. Both of these tubes have a maximum brightness potential about five times that of the shadow mask tube. The mask of the shadow mask tube stops about 80% of the electron stream, making the tube relatively inefficient.

The three color thin-type CRT has an inherent resolution possibility from 1000 up to 2000 lines, making it considerably better than either of its competitors in the display of fine detail. This added resolution potential is due to its simple geometry together with the fact that the green layer, which carries the fine detail primarily, is a single flat phosphor surface with its separate electron gun and focusing deflection system.

Except for a major breakthrough or discovery of an entirely new display method, the CRT will dominate the field of small screen dynamic real time color display for an indefinite time in the foreseeable future.

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3.5 A DISCUSSION OF DIGITAL AND ANALOG TECHNIQUES IN DISPLAYS

Since the early Cathode Ray Tube Displays were utilized only for the display of radar data, the requirements of registration, capability for time sharing, and flicker free display did not exist. With the incorporation of computers into fire control and data processing systems, and the use of precision radar, the requirements imposed upon CRT displays became severe. Where normally analog techniques were satisfactory for deflection voltage generation, new requirements for precision offsetting of sweep origins, display of very low ranges, and precision registration between video and synthetic (computer) symbology placed extreme requirements on the electronic circuitry. This has led to development of digital techniques in order to lessen the requirements on analog circuitry. And, with the advent of inexpensive microelectronic logic elements, additional display functions are being accomplished with digital techniques.

3.5.1 Range Scaling

Figure 3-56 illustrates an analog sweep deflection system. The time-baseramp, derived from the radar trigger by use of an integrator or similar technique, is operated upon by the Sweep Processor to obtain $R \sin \theta$ and $R \cos \theta$. This sweep processor may be a sine-cosine potentiometer, a resolver, or some other device which will convert the angular motion of the antenna and the sweep ramp to a ramp varying as the sine and cosine of the antenna angle, the resultant necessary for the display of a PPI sweep.

Capability for four different range scales and offsetting is shown. With ± 30 volts into the deflection amplifier for full scale deflection, the deflection sensitivity for a twelve inch CRT is 0.183 inches/volt. With a noise pickup on the signal lines of 20 millivolts, there will be a noise disturbance of approximately 0.004 inches on the display; this is considerably less than a spot size and insignificant. However, with the range control set at lower ranges (thus higher gain of the deflection amplifier), the effect of the 20 millivolts of noise will be increased. At the 64 mile range, the noise disturbance will be 0.032 inches, clearly seen and not acceptable. Although the effect of the noise on the lines can be lessened by careful design and the use of differential amplifiers in the deflection chain to take advantage of common mode rejection,

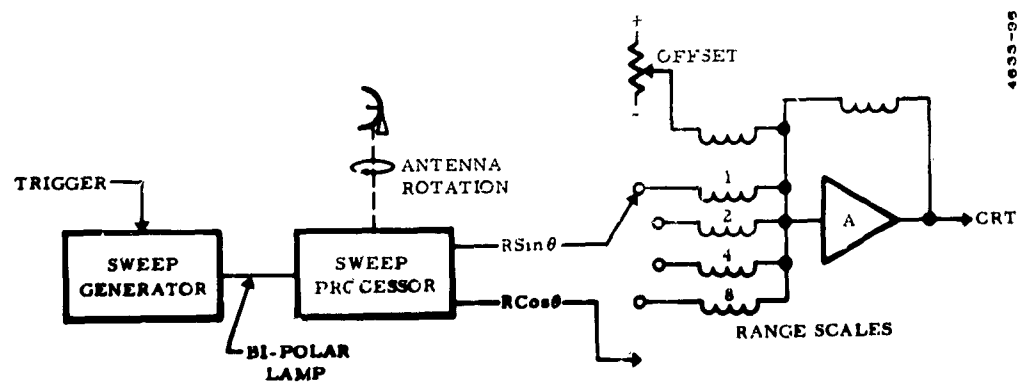


Figure 3-56. Analog Sweep/Deflection System

noise caused by power supplies and ground currents will still result in display noise.

One solution to this problem has been the use of multiple sweep generators, one for each range setting, and the range switching is accomplished by selection of the corresponding sweep rather than a change in gain of the amplifier chain. This is costly but practical for a centered display, but, with offset added to expansion the basic long range sweep must be used and amplified, and noisy sweeps will again result.

Figure 3-57 illustrates a display for both computer-derived data and radar data, using analog techniques. The digital position of the synthetic display data is converted in the digital-to-analog converter; then the selection of the data for display is made by clamping out the unwanted signal. Range scaling and offsetting is accomplished as before.

This technique has been used extensively, but with restrictions. When the radar dead time is sufficient to display all of the computer information, a combined display can be used with no loss of radar information. As the quantity of computer data to be displayed increases, it becomes necessary to interrupt live time for synthetic display. To hold this interruption to an acceptable level, high speed deflection circuitry and symbol generators must be used. One solution has been the use of multiple-gun CRTs, but because of registration errors due to misalignment of the guns and unbalance between the separate deflection systems, this has not been utilized near as extensively as the interrupt technique.

Even with sweep interruption, misregistration still occurs, since up to the range scaling there are separate deflection channels, with the change for unbalance. The clamps used must be high quality, with low offset and very little storage; otherwise erroneous signals are fed into the deflection system. A large number of adjustments with frequent requirement for adjustment is typical of this technique.

Figure 3-58 illustrates a system in which the sweep signal is fed into the deflection system as before, but the synthetic display is range scaled before conversion to analog form, and is fed into the deflection chain with a constant gain. Figure 3-59 illustrates the technique of this range scaling, referred to generally as digital range scaling. Depending upon the position of the Digilog (for digital-to-analog converter) relative to the digital input, the significance of the digits is controlled. Ambiguities result since several points of the overall deflection signal (in digital

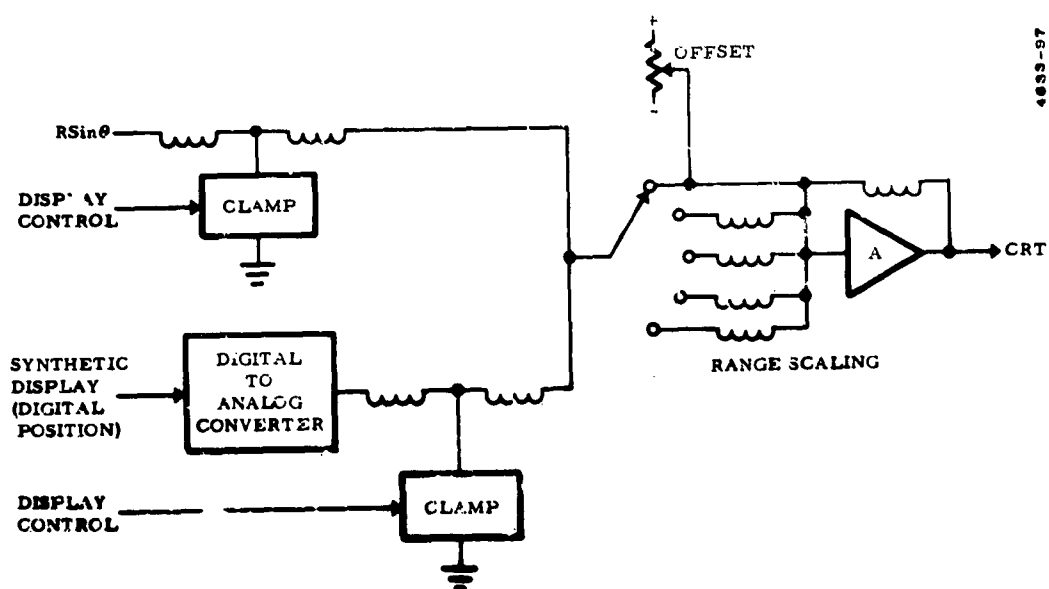


Figure 3-57. Synthetic Radar Display with Sweep Interruption

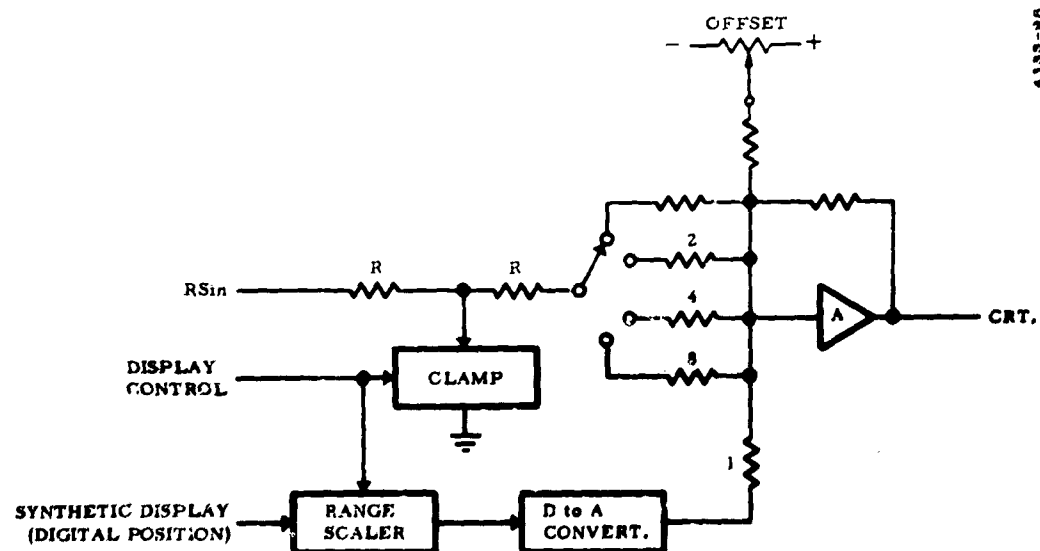


Figure 3-58. Synthetic-Radar Display, with Synthetic Display Digital Range Scaling

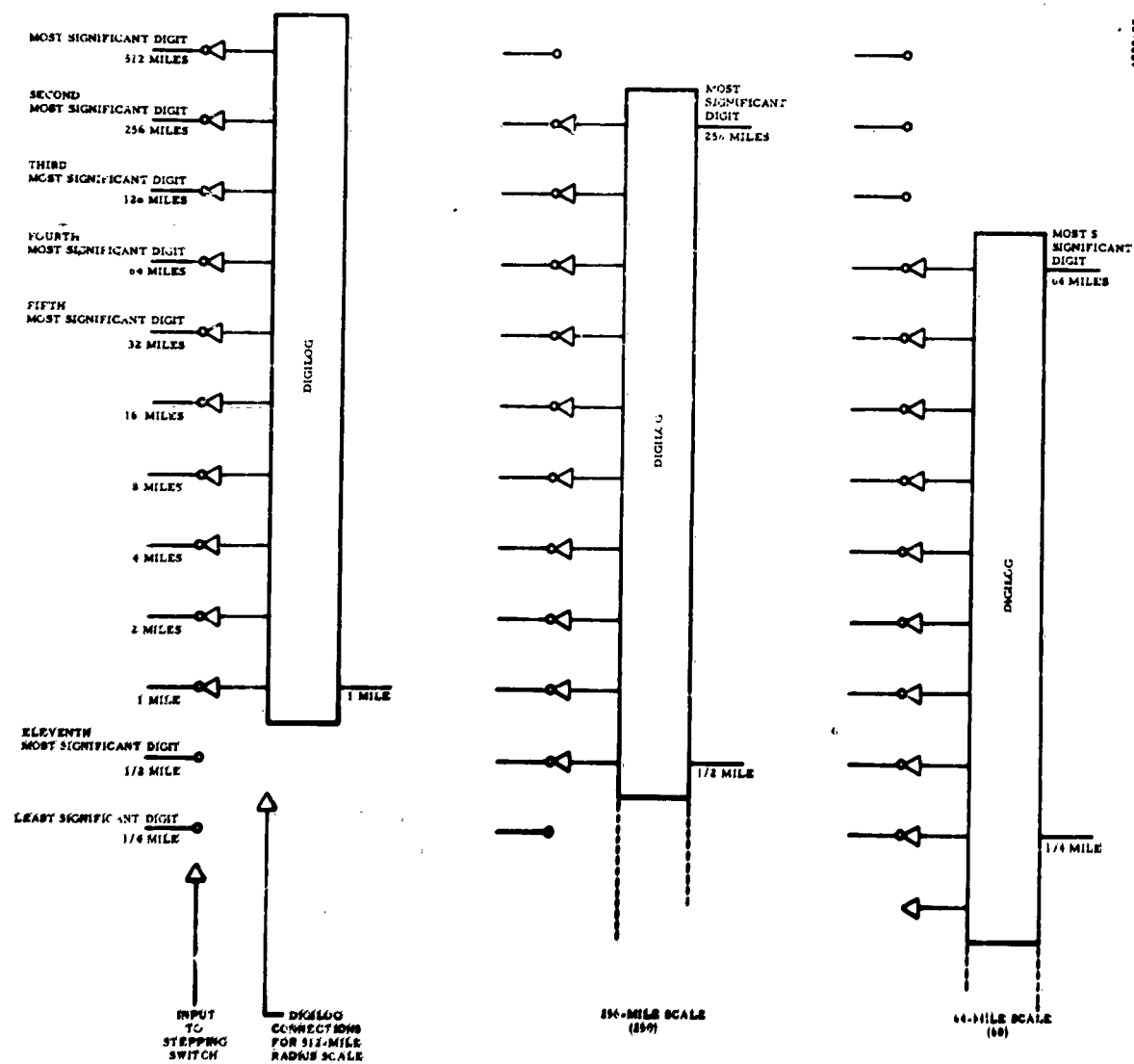


Figure 3-59. Digital Range Scaling

form) will have the same arrangement of the less bits; on lower range scales, where the more significant bits are dropped, this will result in having several display areas superimposed over each other. This is eliminated also selecting the area to be displayed in the intensity chain of the display, and only intensifying the desired area.

Although this digital range scaling offers significant advantages over the analog scaling technique, with the sweep received in analog form it can only be utilized for range scaling the computer-derived data, where the data is received in digital form. An obvious advantage-perfect registration is derived if the same digital-to-analog converter can be used for both radar and synthetic data. Additionally, the selection for display of either sweep derived data or synthetic data can be made digitally, before the conversion to analog form. This eliminates the requirement for precision clamps.

Offsetting can be accomplished by adding the digital number of the desired offset in to the digital definition of the synthetic display. Offsetting with analog range scaling is usually accomplished by adding in a DC level to the deflection system. This technique also introduces noise into the system, unless the DC supply is very carefully filtered.

3.5.2 Digitally-Derived Sweep

As noted earlier, to make optimum use of digital range scaling, the sweep must be received in digital form. A simplified form of a system for accomplishing this is illustrated in Figure 3-60. Antenna position is received from the antenna as a digital code or as a series of pulses (referred to as Azimuth Change Pulses, or ACP), the rate of which is determined by the rate of change of the antenna. These signals are then used to develop a digital signal corresponding to the sine and cosine of the angle of the antenna related to a selected point, usually North. These signals are synchronized to the radar main trigger to change only during dead time of the radar. These signals, together with a real time clock, are fed into the Rate Multiplier. The Rate Multiplier multiplies the clock by the sine (or cosine) of the antenna position; to explain, if the sine is 1.000 (an angle of 90 degrees), all pulses of the real time clock are transmitted. If the angle is 30 degrees (a sine of 0.5000), only every other clock pulse is transmitted. Since the full clock count represents full scale deflection on the CRT, and the sine and cosine are changing together, a digital PPI display is so derived. True, the sweep

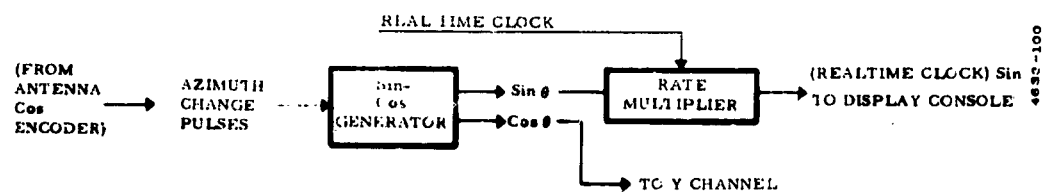


Figure 3-60. Generation of Digital Sweep

moves in discrete steps, but enough steps are used to overlap successive points and the sweep appears as a continuous straight line.

The frequency of the real-time clock is directly dependent upon the resolution required of the display, the number of range scales required, and the rate required of the sweep if it differs from the radar standard used of 12 microseconds/statue mile. As an example, assume 10 bit accuracy is required for a 12" CRT display, this corresponding to 1024 discrete points across the diameter of the tube. With a range scale of 512 miles, the lowest digit represents 1 mile, or 12 microseconds. This specifies the real-time clock frequency, 83.4kc. As the range scale is reduced, the frequency increases; at a 64 mile range scale, the frequency is 666kc. At 2 miles, it is 21.3 megacycles. At range scales below 2 miles, analog techniques must be used until higher speed digital elements than are presently available are developed.

Another problem associated with digital sweeps are switching transients at the steps, resulting in interruption of the sweep display on the CRT. New techniques have been developed to insure symmetrical switching of the circuitry, but at the higher speed even the nanosecond difference in switching times can result in serious sweep disturbances.

Figure 3-61 illustrates a display deflection channel utilizing digital range scaling, offsetting, and display selection, as described.

3.5.3 Line Generation

Lines, to indicate direction of travel, speed, or assignment, are generally required of all CRT display systems. These lines can be generated by analog techniques, using integrators, or can be formed of a series of steps as used to generate the radar sweep previously discussed. To keep the interruption of sweep to a minimum, however, the minimum time is allowed to describe a line. (For electrostatic systems, this is typically 6 microseconds; for high speed electromagnetic systems, 24 microseconds are allowed.)

Figure 3-62 illustrates an analog range generator. The X and Y length of the desired vector are received in digital form, and, on command, an operational integrator is used to form the ramp. This technique has several disadvantages; drift in the reference supply of the integrator will result in an improper termination of the vector. Drift between the

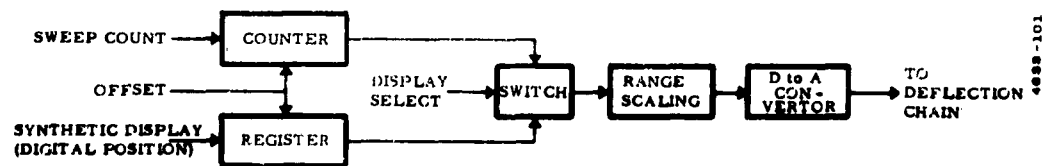


Figure 3-61. Digital Deflection Chain

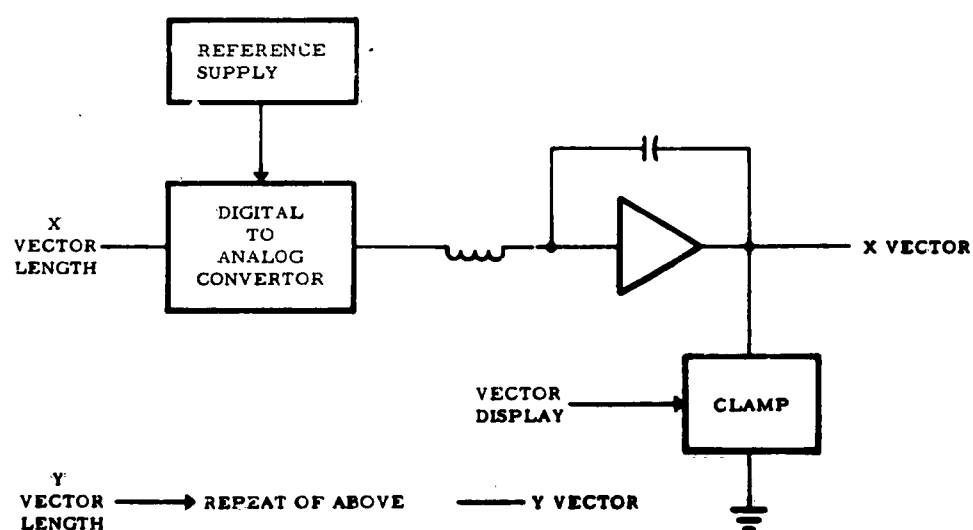


Figure 3-62. Analog Range Generator

integrators of the two channels will also result in erroneous termination. Additionally, the switching of the clamp that controls the vector integration time will, unless carefully controlled, result in a transient disturbance on the display.

The digital technique for line generation has none of the disadvantages cited for the analog technique. However, when there are large numbers of vectors to be displayed, or where time is at a premium, it can be utilized only if high speed digital elements are available. As an example, assume a 10 digit system, as described earlier, and a vector length of one radius. A maximum of 512 steps would be required to describe the vector; to paint this vector in 6 microseconds would require a clock rate of over 85 megacycles, not realizable with available units. If the rate were restricted to a realizable 20 MC, it would take 24 microseconds to paint the vector. At a refresh rate of 30 times/second, each vector will take 0.06 of display time. This is far more than can be allowed in most systems.

Figure 3-63 illustrates a combination Analog/Digital Ramp Generator. In this system, one ramp generator is used for both X and Y axes; thus, any drift in the integrator will be applied equally. The ramp generator is used as the reference to the digital-to-analog converters, effectively multiplying the ramp by the digital value set into the converter. Even this technique does not solve the problems associated with ramp generation, however.

This display of ramps pose other problems. If digital range scaling is used with analog ramp display, the digital number of the ramp must be scaled, but the scaling must be such that a vector which terminates off the display on one range setting must terminate off the display on all range settings less than that (care must be taken to not overscale, as could easily occur.) Additionally, vectors originating off the display cannot be displayed, since it cannot be predicted how they will enter the displayable area. Digital vectors have none of these problems, but the time problem as discussed earlier will usually rule out their use.

3.5.4 Symbol Generation

The major forms of symbol generation that have been used are shaped beam, raster scan, lissajous, stroke, and dot pattern. Of these types,

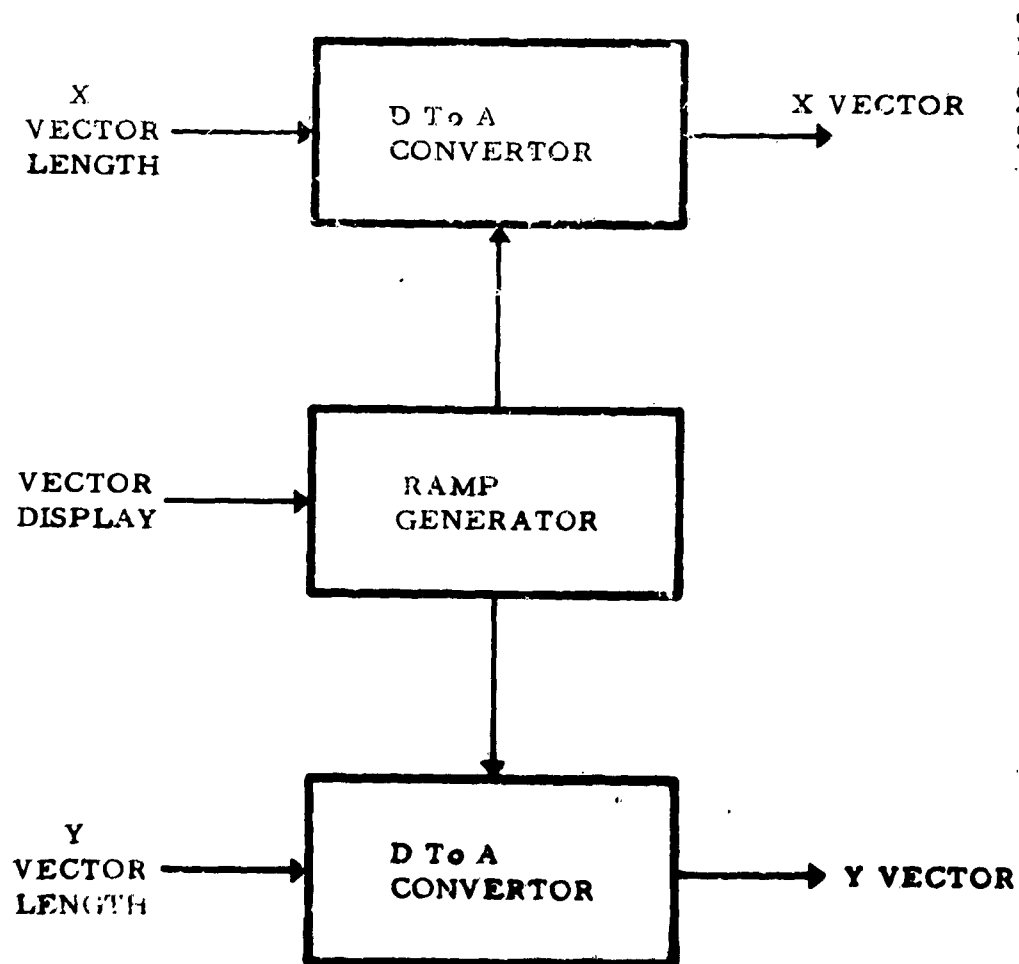


Figure 3-63. Analog/Digital Range Generator

only the last three are basically circuit techniques, and will be discussed here.

The lissajous symbol generator makes use of a basic sine wave which, either by phase shifting, clipping, or other manipulation can be used to form a pattern from which the desired symbols can be constructed, usually with intensity gating. Due to the number of circuits required, and their basic nature, this type of symbol generator is deteriorously affected by drift and phase shift. The frequency used is usually quite low (typically 120kc) to minimize the effects of phase shift, and therefore requires considerable time to describe a symbol (upward of 100 microseconds). It is not readily adaptable to digital techniques, and therefore cannot use readily available integrated circuits.

The stroke generator, as originally developed, was closely akin to the lissajous symbol generator. A family of ramps were developed, and, by selection of these with control of the gain of the amplifier used to sum them, the desired symbol could be constructed. Another variation constructed a digital form of the desired symbol by summing the digital elements, then sent these into an "integrate and hold" circuit to create the final symbol. The first type of stroke generator no more lends itself to microminaturization than the lissajous unit; the second, however, since it makes use of many digital techniques, can be microminaturized. The summing amplifier and integrate and hold circuitry must remain analog, however.

Stroke generators can be made very fast, requiring 0.1 to 0.2 microseconds per stroke. Since the entire unit is synchronized digitally, any drift that can occur will occur in the final stages, affecting the finished pattern as a unit, and will not degrade the symbol. And, since the intensity signal is also derived from the digital clock, this will stay synchronized with the symbol waveform.

The Dot generator can be mechanized using core logic, by resistor summing, or with digital stepping techniques, much as the sweep mentioned earlier is formed. This technique has several advantages over the first two, chief of which is that this generator is completely programmable from the computer while the others require hardware change to effect a change to a symbol or to add a symbol. It can, of course, be completely mechanized using logic elements and thus lends itself readily to microminaturization.

As with the digital technique of vector generation, speed is the limiting factor with the completely digital dot generator. Operating at a reasonable clock frequency of 10 MC, or 100 nanosecond per dot, even a barely acceptable 5×7 dot matrix would require approximately 6 microseconds for a fixed alphanumeric format. By not using a fixed format, however, the average time for alphanumerics can be reduced to less than 3 microseconds. No drift or synchronization problems exist with this technique.

3.5.5 Conclusion

Although, in general, digital techniques require more hardware in their implementation than the analog counterpart, accuracies and freedom from deterioration with age can be achieved that cannot be achieved with analog techniques. With the availability of low cost, high speed, digital, integrated circuits, it is most likely that all of the digital techniques, and the race will be to develop new and simpler digital techniques for those areas where analog techniques are still used. One particular area is in video amplifiers wherein digital video amplifiers are now being developed. Others will follow.

3.6 ELECTROLUMINESCENCE

3.6.1 General

Electroluminescence is the direct conversion of electric energy into light within a phosphor. Whereas the production of light through incandescence involves intermediate conversion to heat, the "cold" emission from an electroluminescent substance depends on its chemical and physical structure. Different forms of electroluminescence were discovered by Lossew in 1923 and Destriau in 1936. The first practical EL lamp was developed in 1950. In 1955, W. Piper*conceived of an EL television display consisting of a phosphor sandwiched between an array of mutually perpendicular conducting strips in matrix form. Needless to say, the CRT still reigns supreme in this field; however active work continues. By 1958, consideration was being given in several laboratories to large EL wall displays for conveying alpha numeric information, target tracking information etc. [6] [3].

More recently, EL bar graph instruments have become available for replacement of the panel type and tape drive indicators for a wide variety of applications, including avionics [12],[13],[14]. Figure 3-64 illustrates an EL bar graph display. Attention is now being directed to the potential application of EL to the dynamic display requirements of avionics, such as the head-up, vertical, and horizontal displays. Figure 3-65 illustrates the format of a vertical display. An even more ambitious goal could include not only such displays in an integrated display panel, but conceivably even the numerous indicators required for monitoring the overall aircraft plant. The flow of information in current sophisticated avionics systems is shown in Figure 3-66 demonstrating the fundamental importance of displays.

Construction

The basic structure of an EL panel display resembles a flat plate capacitor, see Figure 3-67. The phosphor is embedded in a cellulosic dielectric of high dielectric constant (of the order of 20). This mixture is sandwiched between the electrodes. While the electrodes may have any configuration, the crossed grid configuration (two sets of conductors at

*U.S. Patent 2,698,915 issued January 4, 1955

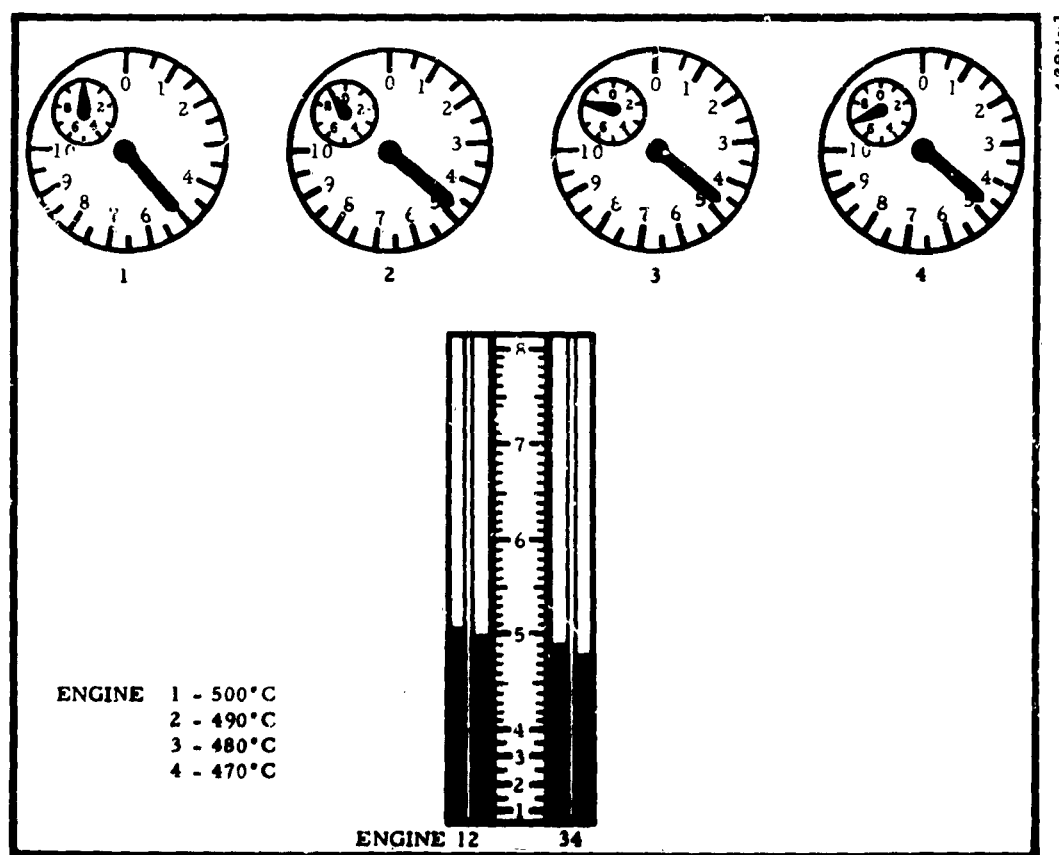


Figure 3-64. EL Bar Graph Display vs
Conventional Engine Instruments

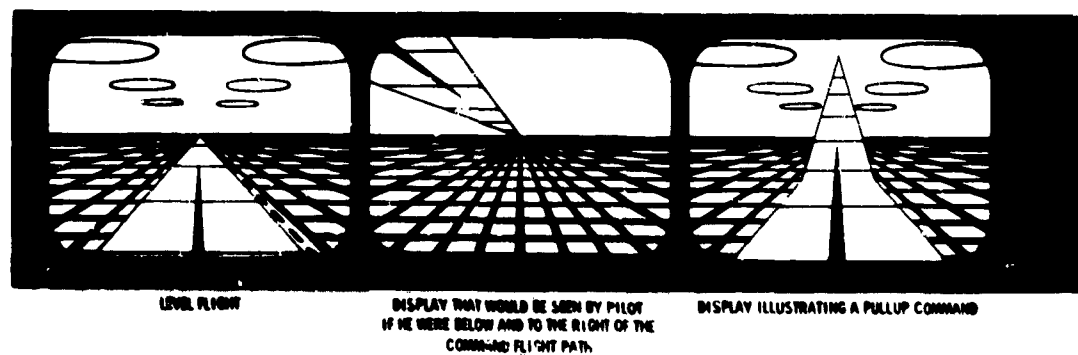


Figure 3-65. Vertical Display

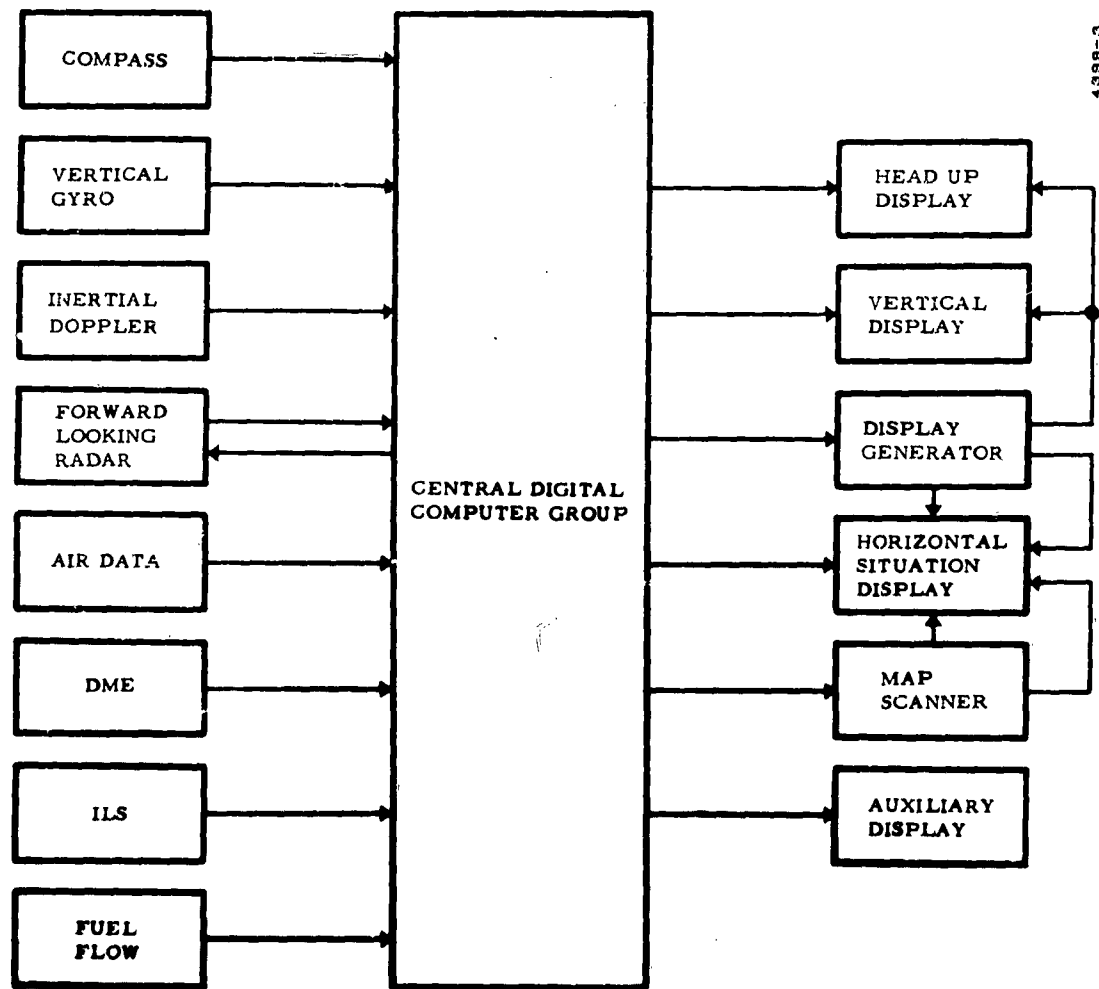


Figure 3-66. Advanced Aircraft Avionic System Showing Sensors/Computer/Displays Interface

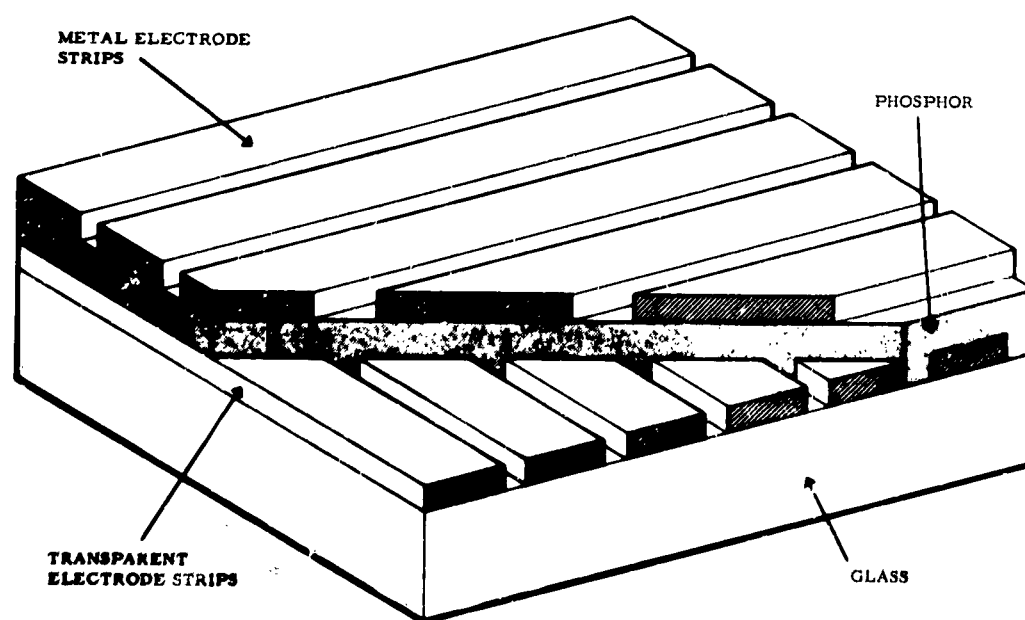


Figure 3-67. EL Display Screen

right angles) is preferred. This configuration is shown in Figure 3-68. The result is a matrix of individual light elements addressable by digital selection techniques. One of the electrode sets must be light transmissive. This is accomplished through the deposition of stannous chloride on a glass or plastic surface. The resultant thin layer is both a good conductor of electricity and transparent.

While a long list of substances, both inorganic and organic display electroluminescence, the most useful present day phosphor is ZnS. Of the three crystal forms of zinc sulfide, hexagonal, rhombohedral, and cubic, the last is the most useful for electroluminescence. The basic phosphor is intermixed with single or multiple activators in concentrations of 10^{-4} to 10^{-3} gram atoms per mole [2]. The activators, in addition to enhancing the EL effect, may be used to produce other changes such as color, frequency response, and voltage response. The most common activators are copper with a halogen activator (usually chlorine), manganese, selenium, or cadmium.

Spectral Composition

Color of the emissions from the phosphors is dependent on a large number of preparational parameters. Two of the most significant are the phosphor firing temperatures and the activators used. ZnS phosphors with the single activator Cu displays blue and green bands when fired below 1000°C . At higher firing temperatures and for total copper contents of 0.5%, a prominent red band is exhibited.

When a second activator, referred to as a co-activator, is added, additional effects on the color of the emission are noted. For example, when copper is the primary activator, and small amounts of chlorine are added, the principle emission is in the green (at about 5200 Å). In the absence of copper, chlorine produces a blue band at 4400 Å. Another example is the addition of manganese to the primary activator, Cu. In this case an orange to white color is produced having the desirable properties of being independent of frequency of excitation over a wide range.

Much of the effort with respect to spectral composition has been to suppress differential color response in phosphors. Uniform frequency response has been long sought and has been achieved in the refining and doping of phosphors such that a modal hue response is achieved.

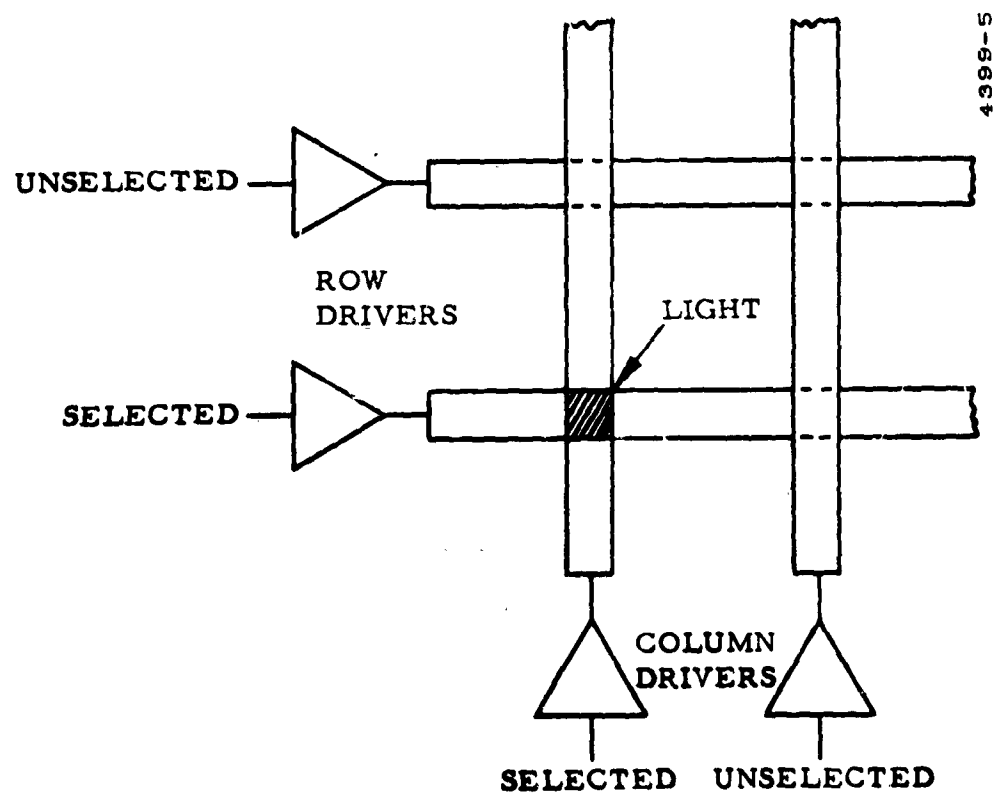


Figure 3-68. Cross-Grid Configuration

3.6.2 Application to Avionics

The potential advantages of a large area electroluminescent display for the cockpit are many. Physically, EL offers a flat, sturdy, self-illuminating display requiring low power. The matrix configuration of the display is ideal for application of advanced production techniques such as printed wiring, thereby eliminating point to point wiring and sockets. These factors all tend toward conservation of vital front panel space. A further production advantage is the inherent ability to segment the display into convenient sized modules.

The cross-grid form of the EL solid-state display has unique digital addressing capability. This permits the adoption of flexible formats as dictated by mission and human factors considerations, and not by equipment limitations. Thus, instead of the present jumbled assortment of front panel instruments and CRT's, a completely functional grouping can be attained. More important, the presentation is under control of the central computer complex and associated automatic monitoring systems. Thus, there is inherent capability for elimination of irrelevant data and unnecessary redundancy.

Digitally controlled EL permits the selection of the most appropriate dimensions for the display of information and data. Numerics and graphics may be portrayed with the same format freedom as in CRT displays. In EL displays incorporating inherent memory, gray scale capability is available. Through the proper mixture of phosphors, a wide range of colors is achievable.

With reference to human factors considerations EL offers several advantages. Its flat format permits easy readout of relatively wide angles. In addition, because an EL display is under complete control of the central computer complex, the data to be displayed may be prequantized as desired and displayed with the optimum scale expansion with essentially zero time delay in so far as the human observer is concerned. This factor is of vital importance in the display of attitude information in a V/STOL, for example. In hover, it is necessary to hold attitude accurately, otherwise translational velocity will be introduced from deviation of the thrust vector from the vertical. It is desirable, therefore, to provide expanded scale display of pitch and roll around the zero reference during hover.

In summary, EL has the potential of achieving a most significant breakthrough in avionics displays, both from a hardware standpoint and, more significantly, from a human factors standpoint. Initial suggestions for su application have already been advanced [16],[20] .

3.6.3 System Requirements

Inasmuch as EL cross-grid technology is under active investigation, it is useful to set forth the system requirements associated with cockpit av onics display systems.

Resolution

The governing factor is the maximum resolution of the eye: one minut of arc. This corresponds, at nominal cockpit viewing distance of two feet to a resolution of 75 lines per inch. Under vibration, the resolution of the eye decreases by a factor 2-5. Thus 75 lines per inch provides adequate resolution for a wide range of viewing distances.

Brightness/Contrast

To assure display visibility over the wide range of cockpit ambients encountered, a brightness specification is customarily applied. Two brightness levels are usually specified. The first, on the order of 1000 foot lamberts, is associated with those displays exposed to high ambient levels of illumination. Examples are the Head-Up display and the Vertical Situation display. A 1000 foot lambert level also represents approximately the state-of-the-art in bright CRT displays. A second brightness level of 150 foot lamberts is specified by MIL STD 411A for displays which are in more favorable ambient illumination environments. This category includes such indicators as warning and caution lights and advisory legends. A further requirement is the automatic proportional control of brightness level as the ambient illumination varies between the daily extremes.

However, it is important to recognize that brightness per se is not a sufficient indicator of display legibility. Display surfaces exhibiting high diffuse and specular reflectance components may well exhibit poor legibility despite high intrinsic brightness. To overcome this difficulty, display engineers are increasingly utilizing contrast ratio as a measurement parameter.

Through contrast enhancement, displays having low intrinsic brightness (such as EL) can be used in daylight ambients found in the cockpit, e. g. 750-1000 foot candles. The practicality of this approach is dependent on techniques which absorb or transmit a high percentage of the ambient illumination incident on the display while not appreciably attenuating the light emitted by the EL.

The improvement through contrast enhancement for relatively thin films can be shown by the following example. Assuming the same color of emitted and background light, contrast is computed by the simple relation

$$C = \frac{B_I - B}{B_I} \quad (1)$$

where B_I is the combined source plus background brightness,

B is the background brightness caused by reflected ambient light.

But
$$B_I = B_{\text{source}} + B \quad (2)$$

$$C = \frac{B_{\text{source}}}{B_{\text{source}} + B} \quad (3)$$

$$C = 1 / (1 + \frac{B}{B_{\text{source}}}) \quad (4)$$

If an absorptive filter is placed at the display surface, the contrast formula becomes

$$C = 1 / (1 + T \frac{B}{B_{\text{source}}}) \quad (5)$$

where T is the transmission factor of the filter.

Assume a contrast of 25 is required and that the cockpit ambient is 800 fl. Formula 4 requires a source brightness of 133 fl., assuming a reflection factor of 0.5 for the display surface. Now if a 30 transmission, reflective filter is placed in front of the display, the source brightness need only be 40 fl for the same contrast.

The use of vacuum evaporated, thin film displays offer additional contrast enhancement techniques. Thin films are optically smooth, and when combined with transparent electrodes, permit optical transmission factors of 30-50 . Thus, if a dark film is placed at the rear of the EL panel between the phosphor and the back electrode the ambient illumination is absorbed. As an example, an ambient source of 1000 foot candles/sq. foot shown directly on the EL film resulted in a background of only 0.1 fl. A second approach would be to further enhance the optical transmissivity of the EL film. In this way the dark absorbing film may be eliminated. This offers the potential for superimposing other information on the display.

Addressing

Of the various digital computer compatible addressing schemes available, the highest economy is achieved through the use of x-y orthogonal sets driven by one-half select principles. This allows a matrix of n^2 switching elements to be selected by $2n$ drivers. Such selection may be conveniently formulated to provide drive to the display a line at a time. This is advantageous from the standpoint of minimizing switching time as compared to individual accessing of each element.

Other requirements on addressing must be imposed. The addressing technique should not produce spurious momentary flickers of light nor perceptible cross coupling. It is also desirable that the input logic levels required be compatible with the low output levels of avionics computers.

Suppression Ratio

The brightness ratio between selected points with full applied voltage and nonselected points with one-half applied voltage is referred to as the suppression ratio. Unfortunately, this definition, taken by itself, is somewhat meaningless in comparing films unless the voltage or the brightness level is specified. This follows from the nonlinear relation between brightness and voltage (using log brightness vs. the square root of the applied voltage, a straight line obtains).

At a specified brightness level, however, a valid comparison can be made. The steeper the slope of the log brightness vs. \sqrt{V} line, the higher the suppression ratio. A high ratio is essential to achieving good resolution and contrast characteristics.

The suppression ratio for EL phosphors is a function of the method of deposition used to apply the phosphor and the dopants chemical composition. The ratio may range to well over 1000 to less than 100.

Storage

To avoid objectionable flicker effects, the EL display panel must be updated at a thirty cycle per second rate or higher. However this rate of data transfer would be too burdensome on the central computer complex. For example, a 500 700 element display would require on the order of 10^7 words per second updating for a one to one correspondence of display element to computer output word. Thus buffer storage must be provided, either externally or integral with the EL panel. This solution is acceptable because natural data rates associated with avionics systems are of the order of several cycles per second maximum.

3.6.4 State of the Art

In this report on the state of the art of large screen EL, the following topics will be emphasized:

Fabrication techniques

Phosphors

Panel design considerations

Storage

Drive

Other addressing techniques

Fabrication Techniques

Two techniques are available, sintering and thin film. Sintering is the more conventional technique in that it has a longer history of use and has been more widely applied. However, potential advantages in the thin film approach is generating considerable current research activity.

1. **Sintering** — The substrate is thoroughly cleaned initially as this is vital to securing adhesion of the phosphor layer. The substrate is then heated to the vicinity of 100°F and the phosphor dielectric mixture is sprayed on with a spray gun capable of producing a fine pattern. Care is taken to produce a uniform deposition. Thickness of the layer deposited ranges from 0.2 mil to 3.0 mil. A thin layer (0.1 mil) of clear dielectric is then superimposed. Subsequently, a baking at 200°F is used to remove all solvents. Back electrodes are then applied to the layer using vacuum deposition of aluminum through a metal mask.
2. **Thin Film** — Phosphor (ZnS:Mn) dielectric mixture is evaporated onto a heated substrate under vacuum conditions of 10^{-6} mmHg. Thickness of deposition ranges from 1-5μ. The temperature of the substrate is carefully controlled, as this factor influences both the establishment of film nucleation sites (from which film growth proceeds) and the incorporation of the activator. Electrode patterns of aluminum are deposited using photoresist techniques and masking. No supplementary heat treatment is required. To improve the dielectric strength of the mixture, various other low conductivity layers are also deposited, including GeO₂ or TiO₂. These layers are of the order of 0.5μ in thickness.

Differences in Sintered vs Thin-Film EL

Thin-film EL exhibits excellent cross suppression. Discrimination ratios between selected and unselected adjacent points of as high as 1000:1 have been achieved. Laboratory samples of 50 lines/inch resolution have been reported. Sintered films require the addition of a non-linear resistance (NLR) layer such as silicon carbide or cadmium sulfide to achieve the equivalent cross suppression. The use of NLR has an added advantage of reducing the effective capacitance of the EL sandwich as seen by the drive circuitry by as much as 10:1. However, there is a penalty attached, namely a reduction in resolution. Thus, NLR cross suppressed sintered panels have typical resolutions of 15 lines per inch. Additionally, the NLR increases power dissipation.

A potential advantage for thin films with respect to avionics application is the inherent film transparency. Thus see-through displays such as the head-up type are feasible as well as applications not requiring transparency.

Phosphors

Scanned EL panels require phosphors that rise rapidly (a few microseconds) to full brightness; require a minimum dwell time (5-20 microseconds) of the excitation voltage to sustain the brightness level during the interframe interval, typically of the order of 30 milliseconds; and exhibit brightness levels of the order of 150 foot lamberts in this mode of operation. Other desirable characteristics include low driving power and inherent cross suppression ratio of several thousand to one. (When used in the cross-grid configuration, this is reduced to the order of several hundred to one due to the intercapacitive element coupling.)

An excellent review of phosphor research for the period 1936-1962 is contained in (2). Figure 3-69 illustrates light output vs pulse voltage for various pulse durations (4). More recent research indicates good prospects for ultimate attainment of the above requirement goals. However, much remains to be accomplished, particularly in the achievement of brightness levels of 150 fl simultaneously with long life. Current lifetimes at such brightness levels are typically of the order of 100 hours. The importance of phosphor materials research was recently demonstrated in another media, color TV, resulting in a dramatic increase in color brightness due to the discovery of yttrium-vanadate rare earth phosphor (YVO_4 ; Eu). In this case, the increase in the red luminous efficiency from 7 to 9-1/2 lumens per watt permitted opening up the previously suppressed blue and green guns, thereby resulting in a greater proportionate increase in overall brightness.

A 1963 investigation of brightness relationships in sintered film panels covering seven phosphor types has been reported (15). Brightness measurements were made using continuous sine-wave excitation. The range of frequency selected was 60, 200, 400, 1000, 2000, and 3000 cycles per second. At each frequency the measurements were made at the following a. c. voltage levels: 55, 110, 220, 300, and 400 (except as limited by breakdown considerations). In addition to the inherent brightness variability between phosphors, the following other variables were found to be significant: phosphor concentration, and thickness. For example, the films exhibited a range of brightness over 3:1 as the phosphor-dielectric concentration was varied by roughly the same amount. A concentration of 6 grams of phosphor to 5 grams of dielectric solvent was found to yield optimum brightness for a wide variety of phosphors produced by three different manufacturers. However, breakdown voltage of the layer decreased with increasing phosphor concentration.

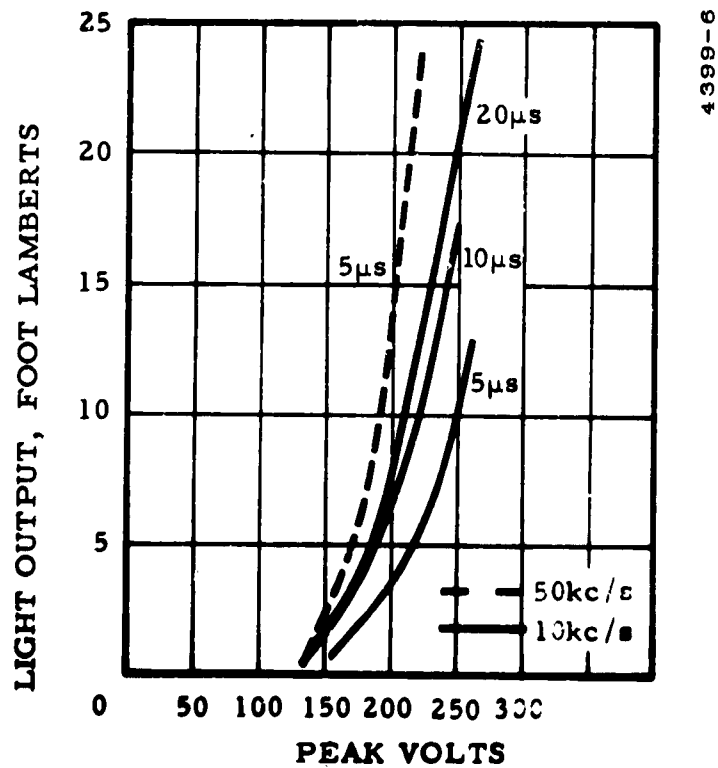


Figure 3-69. Light Output vs Pulse Voltage Duration
From IEE Spectrum-Reference [4]

With respect to thickness, in general the thinner the dielectric layer, the higher the brightness. An increase in the excitation frequency from 1000 cps to 300 cps increased the peak brightness from 100 fl to 200 fl in a bromine phosphor excited by 220 volts. Figure 3-70 illustrates the experimental results for this particular phosphor. It must be stated that these are steady state values of one of the brightest phosphors reported. More typically, phosphor brightnesses under scan conditions are in the range 1-20 fl for both sintered and thin films under conditions compatible with reasonable life times.

Thin-film deposition of phosphor, while highly promising, must at this time be considered in the laboratory stage. No thin film panel, to the writer's knowledge has been subject to typical operational requirements encountered in a large display. However, a great deal has been learned about parameter control required, such as phosphor thickness, oxide thickness (GeO_2), substrate temperature, etc. With respect to size, the deposition of EL films larger than 10 in. x 10 in. has recently been initiated (9) in laboratory quantities.

Panel Design Considerations

Modular design considerations in the construction of EL panels not containing inherent storage has been reported in (18). Module size is limited by processing equipment required to maintain close temperature control during fabrication. Small temperature deviations during processing result in dimensional changes and consequent edge to edge interface mismatching. This, of course, cannot be tolerated in avionics displays with their exacting accuracy requirements. Another factor is the type of driver used for driving the EL elements. The maximum number of illuminated elements that can be driven in a selected line sets an upper limit to the drive line length. A third factor relates to voltage drop on the line, waveform distortion, and phase delay between the coincident selection voltages. This is particularly severe in high resolution panels because of the small cross section, and consequent high impedance of the drive lines. As a result of these considerations, a building block module size of 10-12 inches is considered satisfactory.

Storage

Two approaches to storage have been pursued. In one approach, storage is made an integral part of the EL structure. This is accomplished through the application of materials possessing hysteretic properties to the EL layer. Desirable attributes of this approach include ability

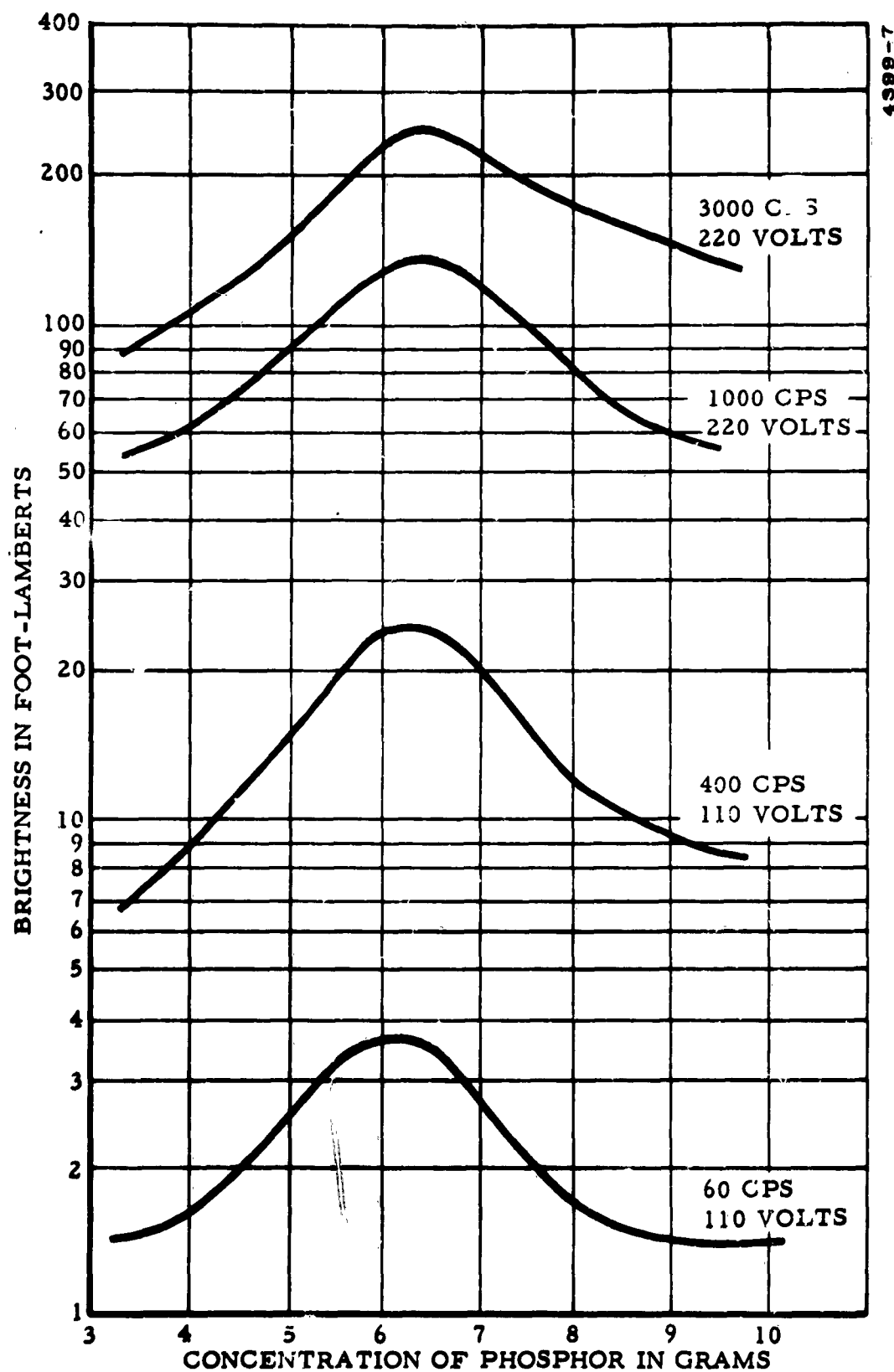


Figure 3-70. Brightness Output as a Function of Concentration of Phosphor-Reference [5]

to achieve wide grey scale range; variable time constants from 2 minutes to 30 milliseconds — opening the door to elimination of separate buffer storage in relatively slow displays (data rates of several cycles per second or less); and complete fabrication through low cost, automated, batch technology. An additional advantage of the integral storage approach is that it is the only technique that maintains excitation of the phosphor throughout the interframe interval. Consequently higher brightness is achieved — a particularly vital consideration for avionics displays.

Early efforts were concerned with electroluminescence-photo conductor (ELPC) combinations with the PC providing decoding as well as an optical feedback path to keep the EL lit after the initial excitation had subsided. However, the EL-PC sandwich exhibited too sluggish a response; hence, at least for large displays, has been discarded. Attention has been centered, since 1958, on various ceramic ferroelectric materials to provide the desired analog storage, decoding, and addressing (6), (8), (21).

A large list of the ceramic ferroelectrics has been investigated including barium strontium titanate, triglycene sulfate (TGS), and most recently, the ternary system lead zirconate stannate titanate. A transcharger for the controlling the EL using the last compound is shown in Figure 3-71. In this figure G_1 represents the row driver and G_2 the column driver. The electroluminescent cell is connected across the balance point of a balanced bridge formed by the four ferroelectrics and the center tapped generator A1. Battery E is used to keep diode D reverse biased. Operation of the circuit is as follows: under balance circuit condition, the four ferroelectrics (FE's) are all polarized in the same direction. Thus generator A1, while switching all four FE's, will by itself not alter the balance condition and no voltage will be applied to the EL segment. To light the EL segment it is necessary to momentarily disable generator A1 and apply pulses from the row and column generators of the polarity shown. These applied simultaneously forward bias diode D, thereby switching the polarization states of ferroelectrics FE and FE₄. When A1 is reenergized, its voltage is applied to the EL due to the resultant unbalanced condition of the bridge. See Figure 3-72.

The brightness of the EL is varied by controlling the degree of imbalance through the magnitude of the row and column select pulses. This follows from the well known relation between brightness and voltage

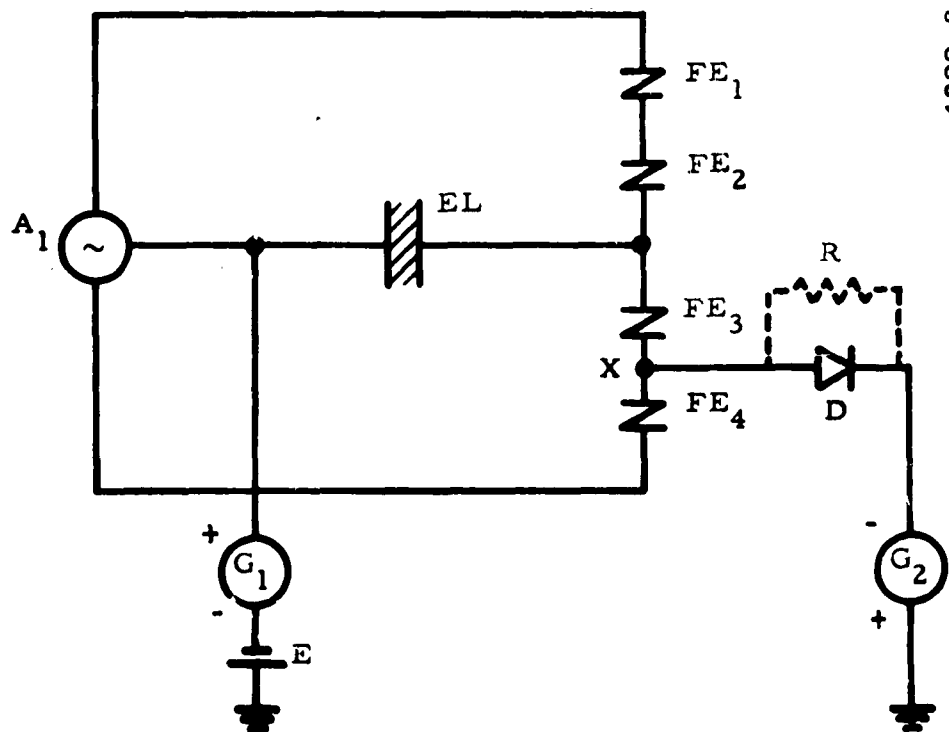


Figure 3-71. Transcharger Circuit-Reference [21]

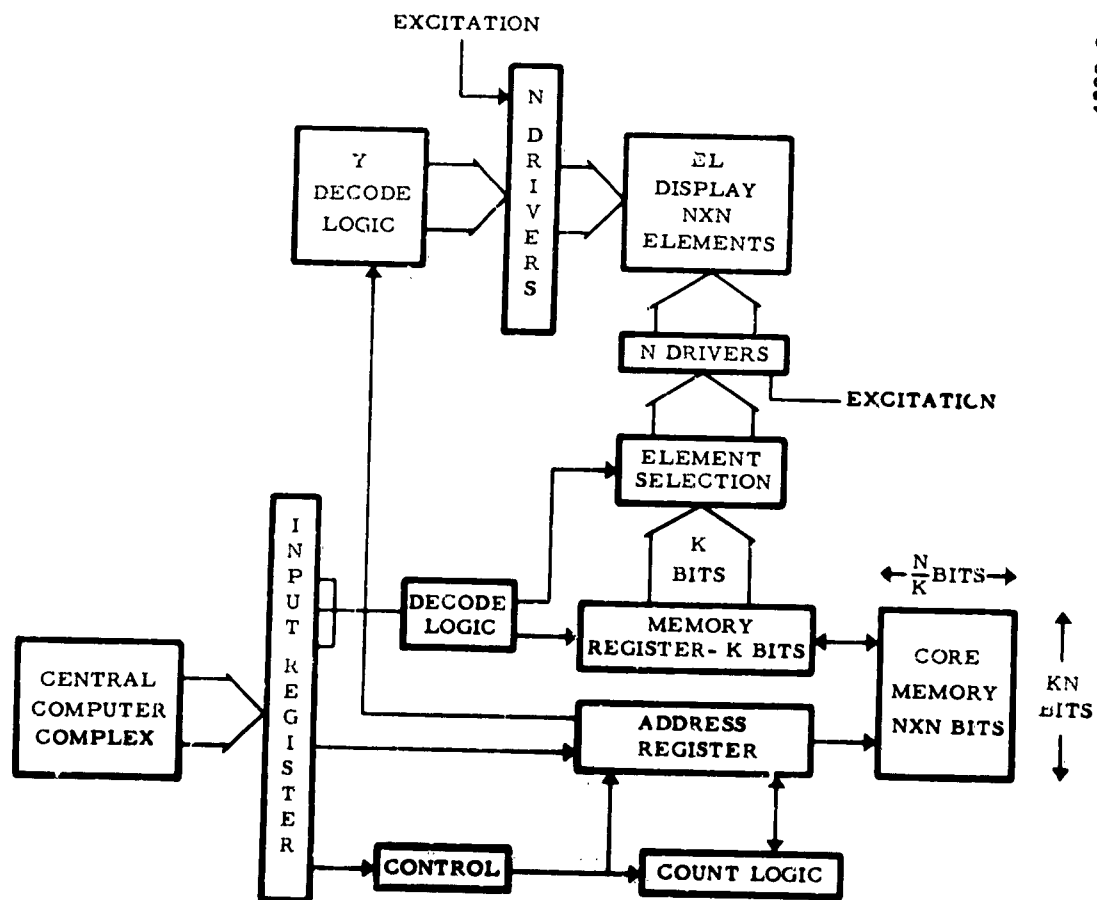


Figure 3-72. Bit Per Element Core Buffer Configuration

for EL:

$$B = A (V - V_o)^n \quad -6)$$

where

B = the brightness

A = a constant

V = applied voltage

V_o = the threshold voltage

n = depends on the physical structure and type of phosphor
(n = 1 to 3 for ZnS)

Using a matrix of 36 EL elements and transchargers arranged in two rows, line addressing was achieved at a frame rate of 30 cps and line addressing time of 30 μ sec. Measured brightness was 6-7 ft-L with a contrast over 100 to 1. Contrast was maintained even when half disturb pulses of 30 μ sec duration and 12.5 kc/s rate were applied (21).

Another storage technique, especially useful for computer generated video applied to scanned displays, utilizes a core or drum memory buffer. The buffer essentially relieves the central processor from the too onerous output rate previously cited. (Typical computer update rates range from 10-40 microseconds per word.)

Various buffer organizations have been proposed. The most straightforward is the bit-per-element configuration wherein a core of the buffer corresponds to an element of the array. This one-to-one correspondence minimizes any format requirements between computer, buffer and display. By multiple memory accesses, the display is effectively driven a line at a time. However, there are the serious disadvantages of a large, expensive buffer - 350,000 bits for our 500-750 display. Alternatively, a drum may be applied if the required display frame rates are not too high. Practical drum structures are not however, in one-to-one correspondence with the display. To keep the number of drum tracks to a reasonable number, each line of the display is segmented to use successive outputs of all tracks. If, for example, 100 drum tracks are used, a display line of the above display is read out in seven sequential steps of 100 bit words.

Organizations more efficient in storage utilization have also been studied (7). These include word per symbol and hybrid storage. In the word per symbol organization, shown in Figure 3-73, storage requirements are reduced by an order of magnitude, since not more than several hundred appear on an avionic display. (Each symbol may be an alpha numeric, a line, a circle, etc.). This saving, however, is achieved at the expense of more complex format and distribution requirements between the buffer memory and the display. The increased formatting and distribution complexity also imposed higher operating speeds on the core storage than in the bit-per-element approach to maintain the same frame rate.

In the hybrid storage approach, a small, moderate speed, word per symbol core memory is used to store the symbol data from the computer. This data is read out at a rate compatible with real time to a symbol generator.

A scan converter tube, see Figure 3-74, is interposed between the symbol generator and the display panel. Data from the symbol generator drives the write gun of the scan converter. The data-modulated write gun electron beam impinges on the nonvisible storage surface of the scan converter, depositing an electron charge pattern which is an exact image of the computer data.

One possible deflection mode of the scan converter appropriate to avionic displays is the use of "jump-scan" deflection for the write gun and TV raster deflection for the read gun. (In modern scan conversion systems both guns may be operated simultaneously and independently with noninterference.) In the jump-scan mode, the write-gun beam jumps to the storage surface position as commanded by the symbol data coordinates. At these coordinates the required symbol is generated in terms of a charge pattern. In this manner, the entire core buffer is repetitively read-out, word by word, and the correct spatial formatting is automatically accomplished.

The unmodulated electron beam from the read gun is directed at the opposite side of the storage mesh in TV raster-scan fashion. A secondary emission is produced from the storage surface representing a TV video signal of the stored image. To achieve compatibility with the line at a time drive required for EL, the video representing one horizontal line of data is accumulated in the information buffer shown in Figure 3-75. After a complete line has been entered, the signal is applied to the

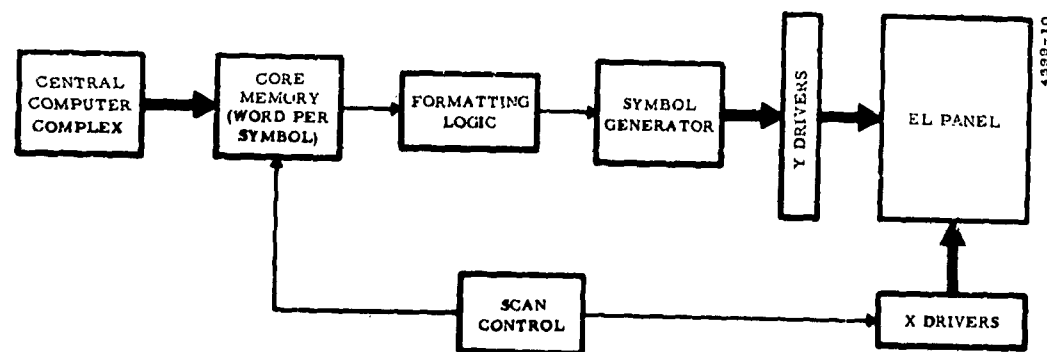


Figure 3-73. Word Per Symbol Storage

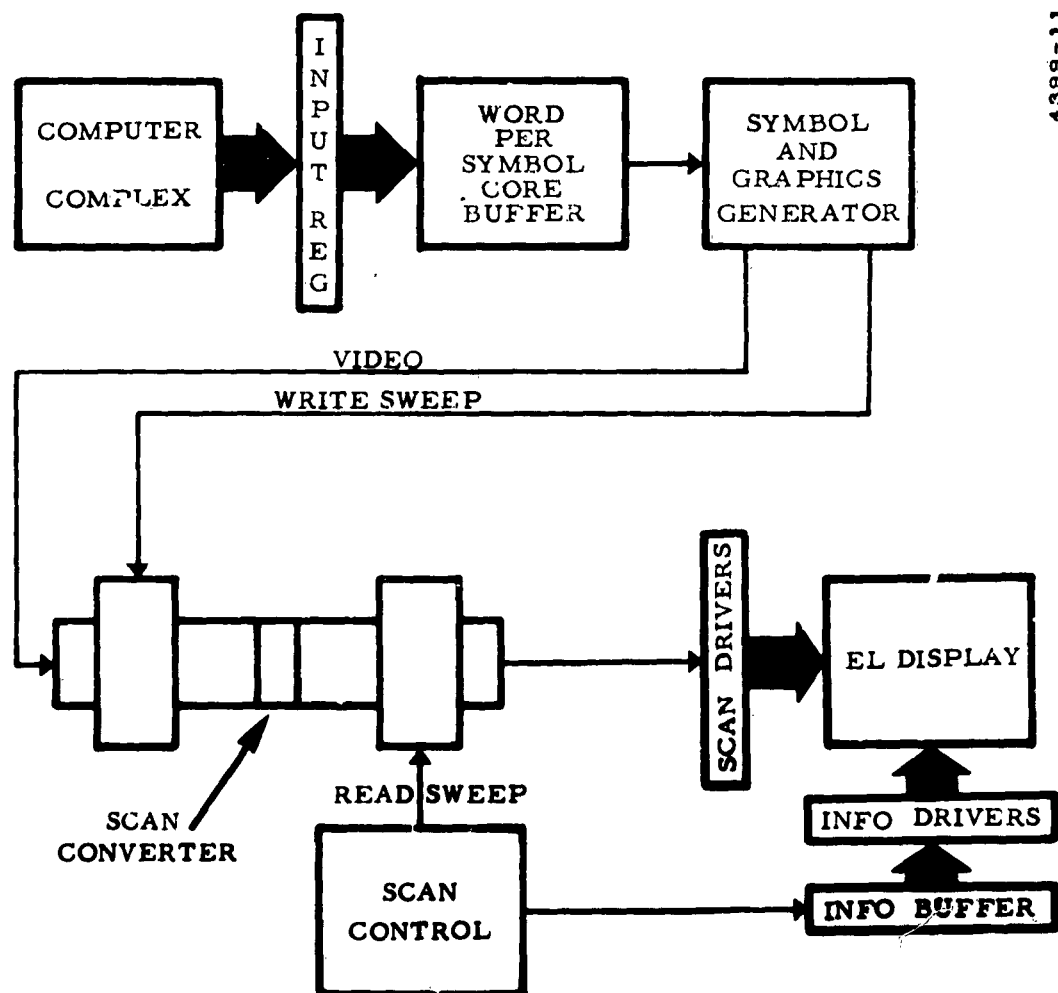


Figure 3-74. Hybrid Storage Display Subsystem-Reference [7]

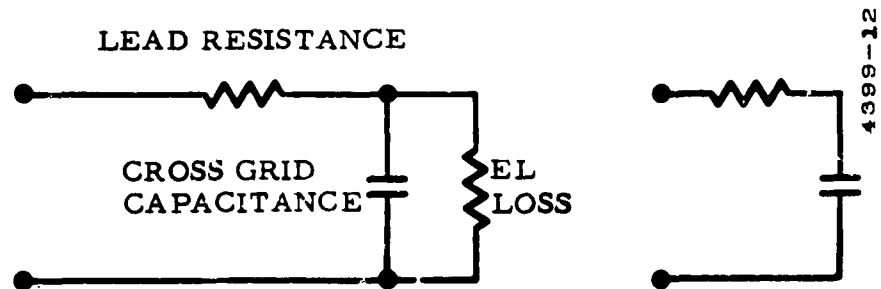


Figure 3-75. Equivalent Circuit of EL Panel Cell

display elements, while simultaneously, the selected line is energized by the scan driver. Thus, the scanning of the storage mesh and the display panel are accomplished in synchronism.

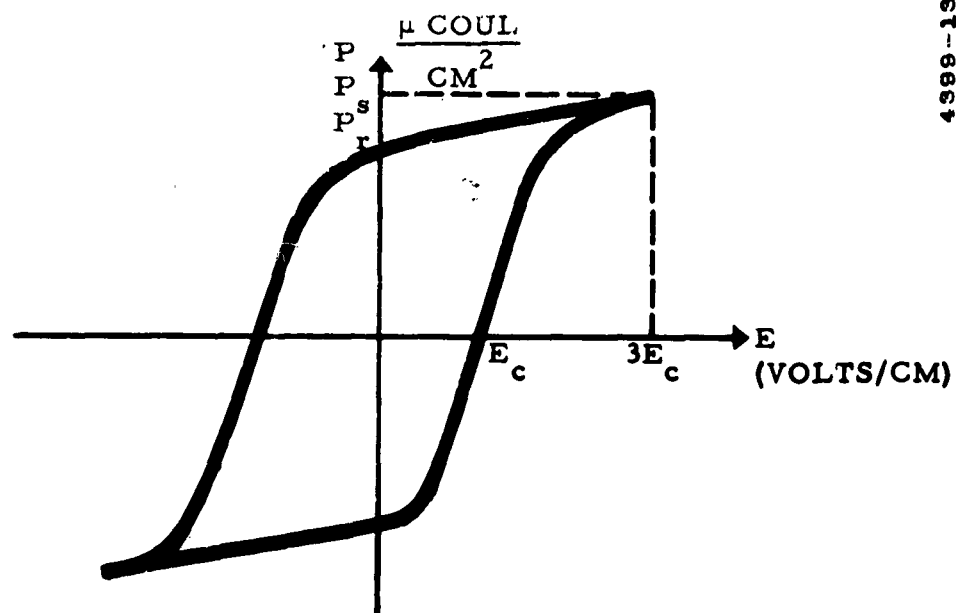
In addition to computer data, the hybrid approach can include maps, sketches, and other types of background data. Any convenient storage media for the background data may be used, such as slides, tape, etc. In this case, however, the write gun of the scan converter is operated in a raster scan mode in synchronism with electronic scanning of the background data.

Problems that must be solved to make the hybrid approach feasible include display accuracy and resolution. Factors in display accuracy include deflection accuracy of the write gun, deflection accuracy of the read gun, and placement accuracy of the storage mesh relative to the read-write electron gun systems. With respect to resolution, a minimum of 1000 TV lines is desired if degradation of chart or map data is to be avoided. Current scan-conversion systems are typically in the order of 500-600 lines, with several of the most advanced claiming close to 1000 lines.

Research and development in the storage techniques discussed above is continuing actively under the sponsorship of several government agencies. Both types of storage may be required for the optimum display, i. e., storage integral with the display as in the case of the transcharger and a buffer store interposed between the computer and the display. New developments in memories including laminated ferrites, MOS (metal-oxide-silicon) systems, and other batch manufactured process may provide the weight, volume, and cost reduction necessary for application to avionics.

Drive and Selection

EL requires high voltages to drive its high impedance, capacitive load. Therefore, it cannot be controlled by standard digital logic. An important advantage of the FE transcharger, in addition to its analog storage capability, is its capability to switch the voltage levels required for EL drive (100-600 volts) within tens of microseconds. The switching action is clear from the charge-voltage characteristic shown in Figure 3-76 and resembles the familiar B-H hysteresis loop of a ferromagnetic material. The parameters shown in the figure are important measures of the FE transcharger capability and include:



4399-13

Figure 3-76. Ferroelectric Hysteresis Loop

E_c = coercive field. Should be as low as possible.

P_s = saturation polarization (measured at $3E_o$)

P_r = remnant polarization

S = squareness = P_r/P_s . Should be as high as possible.

An additional requirement, of course, is the stability of these parameters with life — as yet an unresolved problem.

Other control devices that have been used include NLR, SCR (silicon controlled rectifiers), transfluxors, ferroresonant circuits, etc. However, when consideration is given to the fact that an ordinary 1000 x 1000 element display requires a million switches, sheer economics dictates that some batch production process be applied. To date the highest success has been achieved with the FE. A technique described by Lechner (21) is of interest: a slurry of the ferrocerramic material and a liquid binder is prepared and poured onto a glass substrate. Using a precision coating knife, the mixture is then bladed into a uniform layer. After drying, the layer is peeled from the glass and forming operations are performed such as cutting, punching, etc. The layer is then fired by conventional ceramic firing processes.

The application of the silicon controlled rectifier (SCR) to EL drive continues to receive attention in current research and development programs. A principal reason is the compatibility of the SCR to EL drive voltage requirements. The SCR is a PNP device with a gate electrode as the control element. Electrical characteristics of the SCR are shown in Figure 3-77. Operation is as follows: When gate current is fed to the SCR, it is effectively multiplied by the SCR current gain. (The current gain is equivalent to the gain of a pair of NPN and PNP transistors regeneratively coupled.) This results in the switching of the SCR to the conduction state. If the load current is greater than a minimum value called the holding current, the conduction will continue even though the gate current is reduced to zero because of the internal regenerative feedback. A momentary decrease of the load current below the holding value causes the SCR to switch back to the non-conducting state. This occurs, for example, during the negative excursion of the ac excitation source, in the absence of gate current. However, this mode of operation is limited in speed by the frequency of the source.

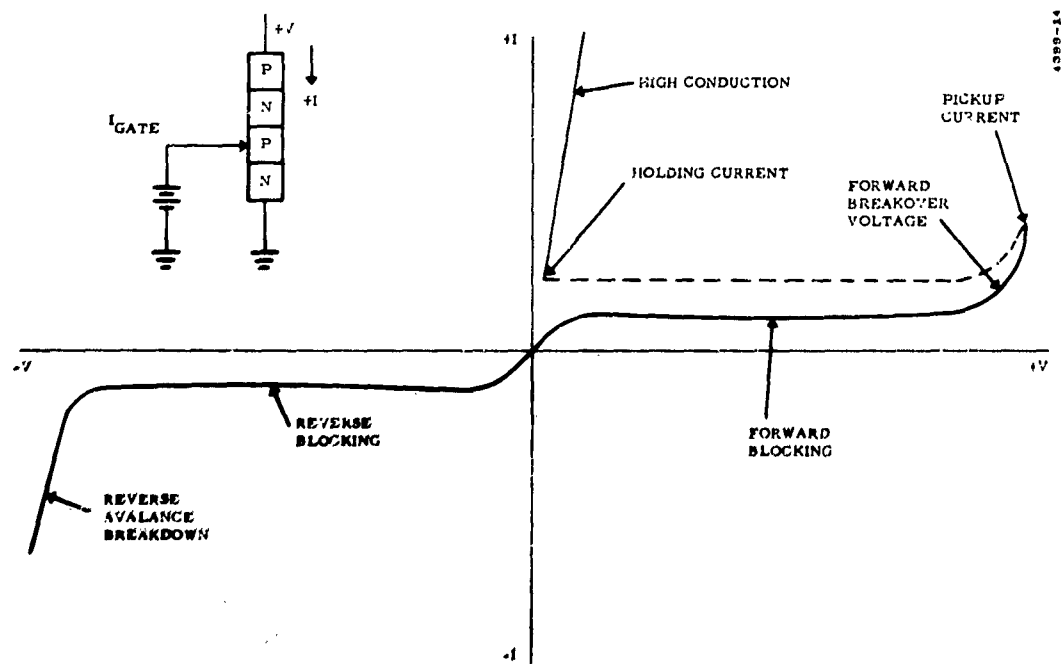


Figure 3-77. Typical SCR Electrical Characteristic

Higher speed operation is achieved if the load current does not enter the high conductance region (i. e., never exceeds the holding current). In this case, the SCR turns off when the gate is driven negative. This mode of operation is normally used for driving the EL and is assured by incorporation of a large series resistor in the anode.

The maximum voltage that may be applied to the SCR anode is specified by the minimum forward breakover voltage (V_{BO}). The V_{BO} ratings of commercially available SCR's indicate that there is no problem in meeting the high EL voltage drive requirement.

When used as an EL driver, the SCR is operated as a simple on-off shunt switch, see Figure 3-78. A simplified switch system schematic is shown in Figure 3-79. Series switch operation is precluded by the lack of isolation between the gate and output. In the shunt mode, a larger resistor is connected in series with the anode. The power supply voltage is shorted to ground through this resistor for each unselected element, with consequent dissipation of power. Increasing R decreases the wasted power but, unfortunately, also reduces the voltage applied to the selected line through voltage divider action. Another limit on the maximum series resistance is imposed by the shunt capacity of the cross-grid line. This is typically of the order of 100 picofarads. The impedance associated with this line capacity again causes voltage divider action when the SCR is open. For an ac drive source, the supply voltage to drive the line would have to be increased to compensate for the reduction in voltage. Also note that the drive is frequency dependent. A final consideration on the maximum series resistance value is the time, delay associated with blocking of the SCR for a selected line. The time constant associated with this delay is

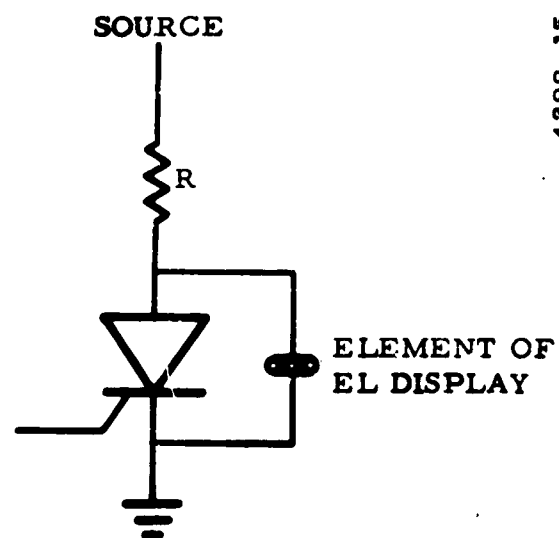
$$T = R (C_{SCR} + C_{cross\ grid})$$

For

$$R = 100K, C_{SCR} + C_{cross\ grid} = 200\ pf$$

$$T = 100 \times 10^3 \times 200 \times 10^{-12} = 20\ microseconds$$

To this value must be added the inherent delay of the SCR itself, of the order of 10 - 20 microseconds. This latter delay is due to stored charge in the two base regions when the SCR is in a conduction state.



4399-15

Figure 3-78. SCR Shunt Drive Circuit

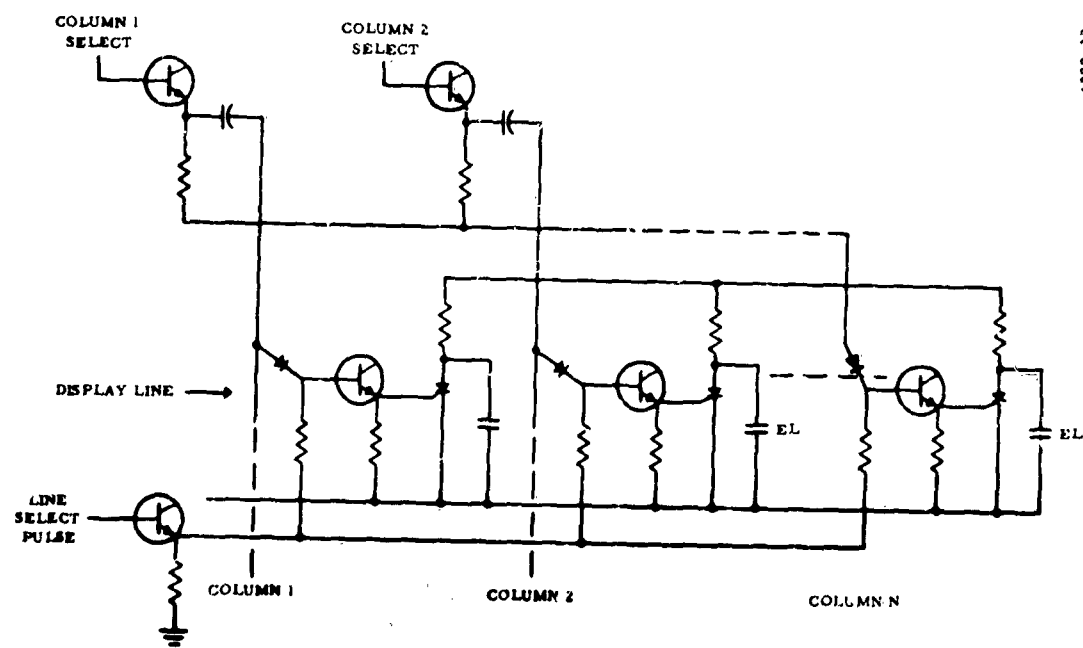


Figure 3-79. Simplified Schematic of Switch System

A minimum value on the series resistance is set by the fact that the gate current to saturate the SCR increases as the anode resistor is decreased. For reasonable gate power (10 - 50 milliwatts), the anode resistance will be 50K ohms or greater.

A final consideration relative to SCR concerns development state and cost. Improvements are being made to SCR as witness the recent introduction of planar technology to their fabrication. This has resulted in improved sensitivity and reduced shunt capacity. With respect to costs, these have dropped from the \$40 - \$50 level to the \$20 level.¹ This of course, is still prohibitive for million element arrays.²

Other Addressing Techniques

Addressing technique based on the cross-grid structure have been described above. Difficulties with these addressing schemes have also been cited, including complexity of the drive equipment and/or high speed drive requirements for reasonable frame rates. A technique potentially overcoming these difficulties was reported in 1962 (19), though no further application to date is known.* This method used the combined properties of piezoelectric ceramics (lead zirconate titanate) and electroluminescent materials. Elastic impulses propagating across a piezoelectric layer produce localized electric fields. Interaction of these fields with the contact EL layer produces light. Through application of the proper voltage waveforms to the x and y axes, a scanning action may be produced enabling the illumination of any selected point of the display. The resultant scanning action is illustrated in Figure 3-8 and 3-81. The similarity to a CRT deflection system is evident with attendant economy in hardware.

The use of Ga As in a PSIN diode configuration has recently been recently proposed as a high speed addressing technique for EL-PC [23]. The PSIN, when electrically addressed, emits light which in turn addresses the EL-PC. Inherent memory is provided in the usual fashion by the EL-PC combination. Speeds accommodating frames of 2000 lines at 30 frames per second appear relizable.

¹A recent personal communication indicates that these may be approaching unit costs of \$2 as a result of fabrication process improvements.

²Would require 1000 + 1000 switching elements for a square matrix in either the series or shunt switching configuration.

*Further results to be reported at the Ultrasonic Symposium of the IEEE, December 1-3, 1965 - personal communication from Mr. S. Yando.

SWITCH MOMENTARILY
CLOSED AT $t = 0$

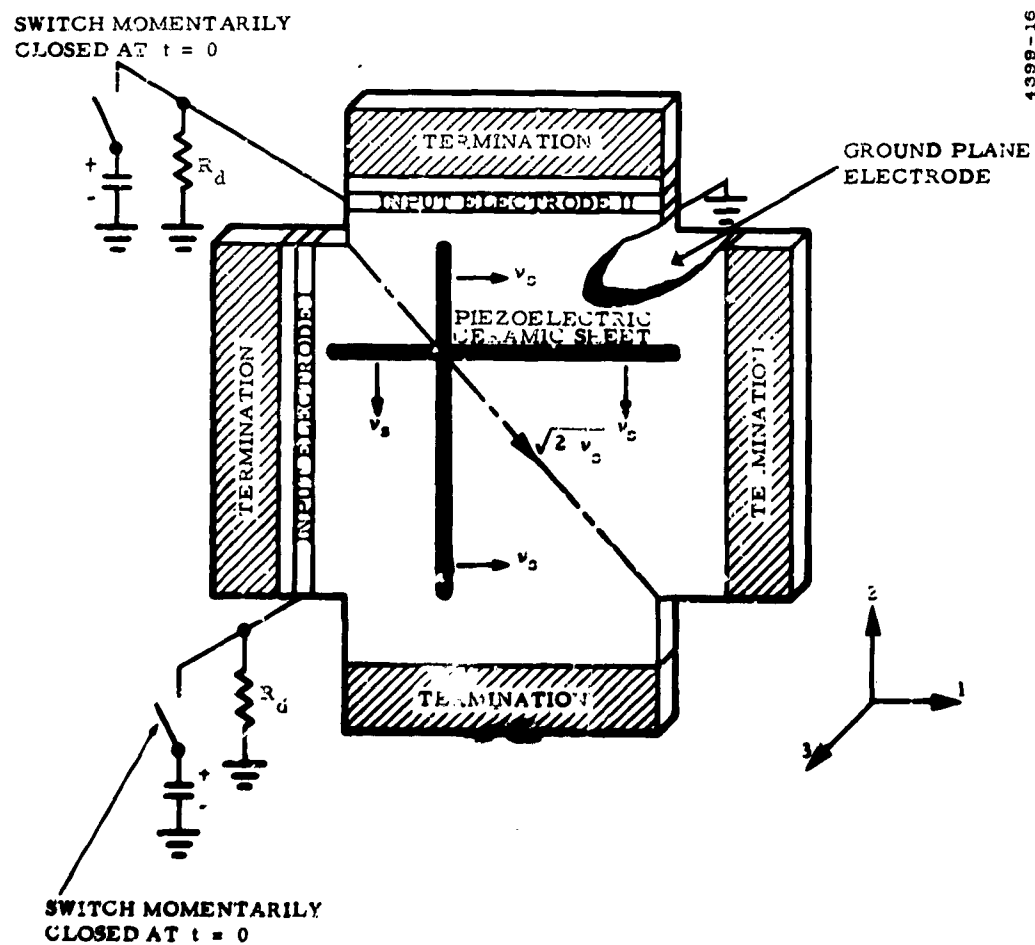
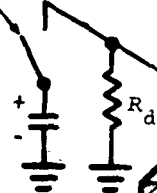


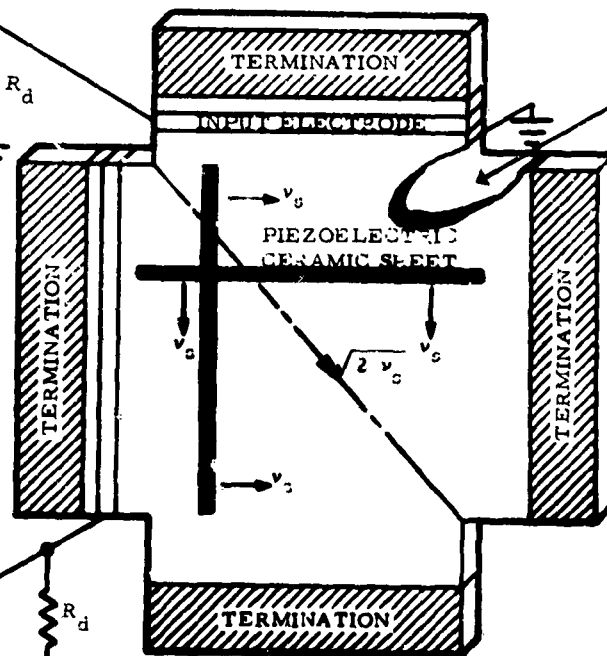
Figure 3-80. Fields Produced by Two Simultaneously Launched Orthogonal Elastic Pulse-Reference [19]

SWITCH MOMENTARILY
CLOSED AT $t = 0$



4388-17

GROUND PLANE
ELECTRODE



SWITCH MOMENTARILY
CLOSED AT $t > 0$

Figure 3-81. Fields When One Pulse is Delayed

Voltage level required to address the PSIN is a function of addressing pulse rise time. The higher the rise time, the higher the required voltage level. For example, at a rise time of 3.5×10^8 volts per second, PSIN switching occurred over a range of 175 volts down to 8 volts minimum.

The photo-conductor material used is CdSe. The PC is fired on a glass substrate and subsequently electrically interconnected with the EL phosphor. The EL layer is of conventional design. Over all resolution of 20 line/inch is obtained, limited principally by the PSIN array density.

Finally, there is the possibility of electron beam or laser addressing schemes. Both offer high frame rates at, however, relatively low brightness levels at this time.

3.6.5 Advances Required Over Current State of the Art

From the standpoint of avionics display media, EL has two major applications. First is the replacement of current panel displays containing meter, digit readouts, tape drivers, etc., with a computer controlled EL panel. The advantage to be derived from this approach have been cited in subsection 3.6.2. The ferroelectrics - EL batch technology, as we have seen, offers an excellent solution to this requirement. At this time, numerous difficulties exist with batch processing of FE, such as warping, cracking, and aging problems. Further work is required with respect to optimum fabrication technique and exploration of other ceramic ferroelectrics.

With reference to the EL cell, the chief improvements required are improved legibility and longer life. As previously indicated, two alternate routes to achieving increased legibility are higher brightness and/or higher contrast. While higher brightness is achieved by higher voltage or frequency (cps) of drive, this approach is ruled out because of the inverse relationship between these variables and life (4). The other hope for higher brightness is improved phosphor materials, though little has been forthcoming from this approach despite extensive past research.

On the other hand, highly promising results have been reported with so-called high contrast techniques (22). Through the use absorption, interference and polarization phenomena, the contrast achieved is expressed by

$$C = \frac{1}{1 + T^2 (B/B_{\text{source}})} \quad 7)$$

(compare to equation 5). With a filter having a 35% transmission - 2% reflection factor, EL display contrast of 30% and 25 fL intrinsic brightness was maintained in an ambient of 955 fL. For the same contrast, a source brightness of 204 fL would be required without filtering.

The contrast improvement through use of thin film EL were previously mentioned (see discussion on Brightness/Contrast). A further advantage of the films is the potentially higher brightness coupled with higher resolution. These qualities have been demonstrated in the research laboratory. If they prove realizable on a production basis, then film EL will be a leading contender for advanced display applications.

The increasing level of support being given to EL research affords excellent prospects that the post 1970 cockpit will be equipped with computer controlled EL indicator panels. However, with respect to the dynamic display requirement, typically provided by CRT's for various situation displays, more fundamental difficulties exist. First, an economical solution to the memory requirement posed by high scanning rates must be developed. A true batch memory would offer one attractive solution to this requirement. Most optimistically, such memories must be considered in the development stage. Along with the improvements in brightness, life, and drive circuitry discussed above, an improvement in resolution is also required. Typical EL cross-grid panels are 25 lines per inch, whereas to compete with CRT technology, this figure should be increased to 100 lines per inch. This, of course, simultaneously compounds the problems associated with memory, addressing, drive, and packaging. The cost aspect also must be considered. Solid-state display must approach the equivalent life cycle

costs associated with the highly advanced CRT technology. That is to say, where initial costs are higher as is likely to be the case, these should be offset by longer life, lower maintenance, etc. From a consideration of the technical and economic objectives, it is evident that many obstacles remain to be overcome.

A good idea of the current state of the art may be gained from a recent study by Litton Systems, Inc. of an avionics display application. While the specific hardware was not constructed, sufficient information was obtained to place a high confidence in the feasibility of the system design. The electroluminescent display panel considered was a thin film type currently being fabricated by Sigmatron, Inc. The buffer memory requirement was easily met by a core memory configuration currently used by Litton in its line of avionic computers. Organization of the memory was in the bit per element configuration described previously and consisted of 4096 words of 64 bits each. The word length was selected on the basis of the required display frame rate and convenient memory cycle time parameters. Line at a time drive was the excitation mode selected. A detailed block diagram of the complete system is shown in Figure 3-82. Other parameters of this display study were as follows:

1. Display - The display is assumed to be 10 inches square with 512 lines on each side, giving 262,144 display intersections. The resolution is thus 51.2 lines per inch.
2. Display Memory - A DRO core memory provides the data storage requirements for this display interface. 4,096 - 64 bit words are read in parallel. The basic cycle time for the memory was 1.714 microseconds.
3. Dwell Time - The dwell time is defined as "the period of time any display intersection, or group of intersections, being continuously energized." The assumed dwell time is 5 - 9 microseconds.
4. Frame Rate - The definition of frame rate is the reciprocal of the period of time it takes for one scan of the 262,144 display points. The frame rate assumed for this mechanization was 60 - 83 frames/sec.

5. Computer Update Rate — The definition of computer update rate is "the reciprocal of the period of time between data transmissions from the computer." The detailed interface design assumes a maximum data transfer rate of once every 24 microseconds or 416 kc. (Note: this establishes the maximum rate at which new data can be introduced.)

Utilizing avionics packaging the resultant volume requirement for a display meeting these specifications was assessed as follows:

Electroluminescent display panel (12 in. × 12 in. × 2 in.)	288 cubic inches
Ferrite Core Memory	48 cubic inches
Memory Electronics	400 cubic inches
Input register, integrated control, and logic circuitry and cabling	<u>128 cubic inches</u>
TOTAL (12 in. × 12 in. × 6 in.)	864 cubic inches

The memory electronics, as can be seen, was the largest volume consumer. For the memory electronics, flat pack layout of state of the art IC's were used. Considerable reduction can be expected in this area as advances are achieved in integrated circuit technology.

3.6.6 Conclusion

Increased future use in the cockpit of EL to instrument panel displays is assured by recent improvements to display legibility through high contrast techniques. Advantages of these displays include instantaneous scale factor change, adaptability to both digital and analog inputs, ruggedness, and flat form factor requiring little space.

Key technology improvements are required if EL is to find use in large avionic displays such as the horizontal or vertical situation displays. These include the availability of a batch-fabricated device incorporating the necessary properties for addressing, drive, and interframe memory; the availability of a batch-fabricated data buffer to reduce I/O traffic between the computer central and the displays; and improvements to the EL panel per se, including viewability, resolution (75-100 lines/inch), and life.

The emphasis on batch-fabrication in the above stems from the fact that only by highly automated fabrication techniques can large EL panels compete, from a cost standpoint, with the highly perfected CRT art.

Solution to the data buffer problem seems assured because of major effort underway by the computer industry in both ferrite and integrated circuit approaches to batch memories. With respect to resolution, the requirements have been attained at the experimental level. Additionally, government sponsored programs in both EL and associated drive and selection have achieved reasonable progress to date. These facts warrant an optimistic attitude toward attainment of large, computer controlled EL displays for the cockpit environment.

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3.7 FIXED FORMAT DISPLAYS

For the purposes of this report, a fixed format display is one in which a change of format must be accomplished by a physical operation rather than by electrical control or programming. For example, if it is desired to add a column to a tabular display formed by an array of cathode glow tubes, more tubes must be added to the board. The changing of the display by merely changing the headings of the columns would not be considered a change in format, but only in information content.

It can be seen that it is not merely the fixed location of display elements that determines a fixed format since the matrix display, such as a large screen electro-luminescent display will also have fixed element locations. However, the large number of these elements and the flexibility of control makes change of format feasible.

Thus, the line of demarcation between flexible and fixed format is not easily determined. The usual manual status board is of relatively fixed format due to the permanently inscribed column and row lines. A plain blackboard on which these lines may easily be drawn and erased would provide a flexible display.

3.7.1 Discrete Readout Indicators

These devices are also often called digital readouts since the most common characters displayed are numerics. This group of devices may be conveniently divided on the basis of the intensity modulation principle into three classes: (1) Light-reflecting (electro-mechanical devices, (2) Light-transfer devices, and (3) Light-emitting devices. Almost all the reflective devices utilize electromechanical character selection and are often classified as electromechanical devices.

Electromechanical Devices

There are several varieties of readouts within this class but the basic principles are similar and quite simple. These common features as shown in Figure 3-83 are: (1) A viewing window, (2) A mechanical component (drum, tape, stack of plates, etc.) with the desired characters imprinted on it, (3) An electrically actuated mechanical device which positions the desired character within the viewing window.

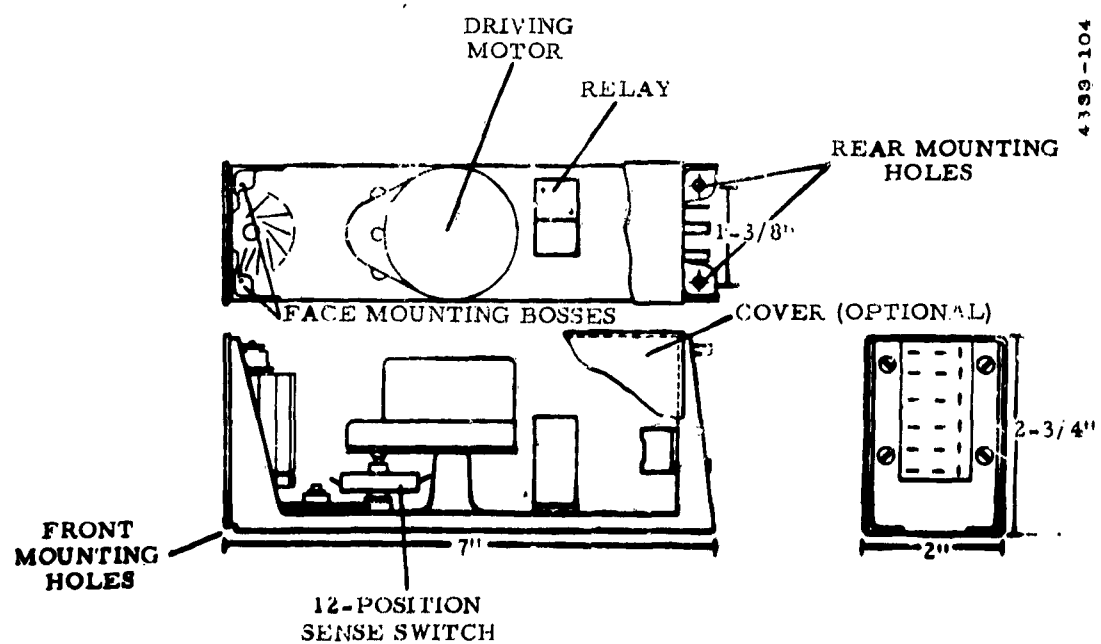


Figure 3-83. Book-Page Type Readout

When only numerics are required a relatively small diameter drum (approximately five times the character height) is sufficient. If alpha-numerics or a large number of symbols are desired, a drum will require excessive panel space and a tape is then preferable, thus extending the unit further behind the panel.

Another means of presenting a large number (up to 36) of characters is a system which utilizes unconnected plates. Each plate carries one character (or even a multi-character message) and has guide pins which follow grooves in the mounting supports under control of a cam. By this means a selected character plate is positioned in front of the viewing window. The stacking of the individual plates results in a very compact unit.

There are several types of drivers used for these displays. They can be positioned by either a servo drive utilizing an encoder attached to the same shaft or by a stepping motor with position determined by the number of pulses applied. In addition, a drum has been used as the rotor of a multipole positioning stator. The drum lines up with the energized pole and is maintained in that position, after power is removed, by a permanent magnet detent.

Another type of electromagnetic display utilizes several moving elements to build up a character from line segments such as the seven segment pattern utilized for numerics.

Each segment is controlled by a rotor and can be set (latched, in "on-condition") by a set signal applied to the corresponding solenoid. This can also be made as a momentary (non-storage) display by eliminating the latching feature. A display of this type with 14 segments permits display of alphanumerics. Probably, the most attractive characteristic of these electromagnetic displays is the inherent, nonvolatile, memory-by-inertia (or more positively by detent). Another good feature is the presentation of each character in a single front surface viewing plane which provides for wide angle viewing and high readability. However, these devices are relatively slow with operating times in the range of 0.1 to 1.0 seconds. In operation with computer input, a temporary storage is required to avoid excessive interference with the computer input/output functions.

The devices described so far all position the desired character and leave it fixed during operation. A device operating on a different

principle illustrated in Figure 3-84. Operation consists of rapidly scanning all the characters past the viewing window and flashing a strobe light when the selected character is at the viewing window. The repetition rate is made high enough to provide a flicker free display. This system, of course, does not have the inherent nonvolatile memory of the other devices previously described.

All of the electromechanical devices are relatively bulky in relation to the size of the displayed character.

Light Transfer Devices

The principle of operation of these devices involves a light modifier between a light source and the viewer (Figure 3-85). The modifier acts upon the light to produce an output shaped to the form of the desired character.

The transfer device may utilize transmission or reflection and in addition may involve magnification and projection.

1. Edge-Lighted Display

One of the first Light-Transfer devices used was the edge-lit plastic plate. When a sheet of acrylic plastic is internally illuminated by introducing light into an edge, light is emitted from any scratch or other discontinuity in the flat surface. This light is very bright compared to the light emerging through the smooth portion of the surface. A decimal readout of this type has 10 plates (with a single digit engraved on each) stacked one behind the other. Each plate has its own light source which may be turned on selectively to display the corresponding digit. The legibility of this type of display is good, but the viewing angle is restricted since the digits are not all displayed on the same plane.

2. Projection Type Digital Indicator

As shown in Figure 3-86, there are four essential components in this device: (1) light source, (2) character shaping mask, (3) lens system, (4) viewing screen.

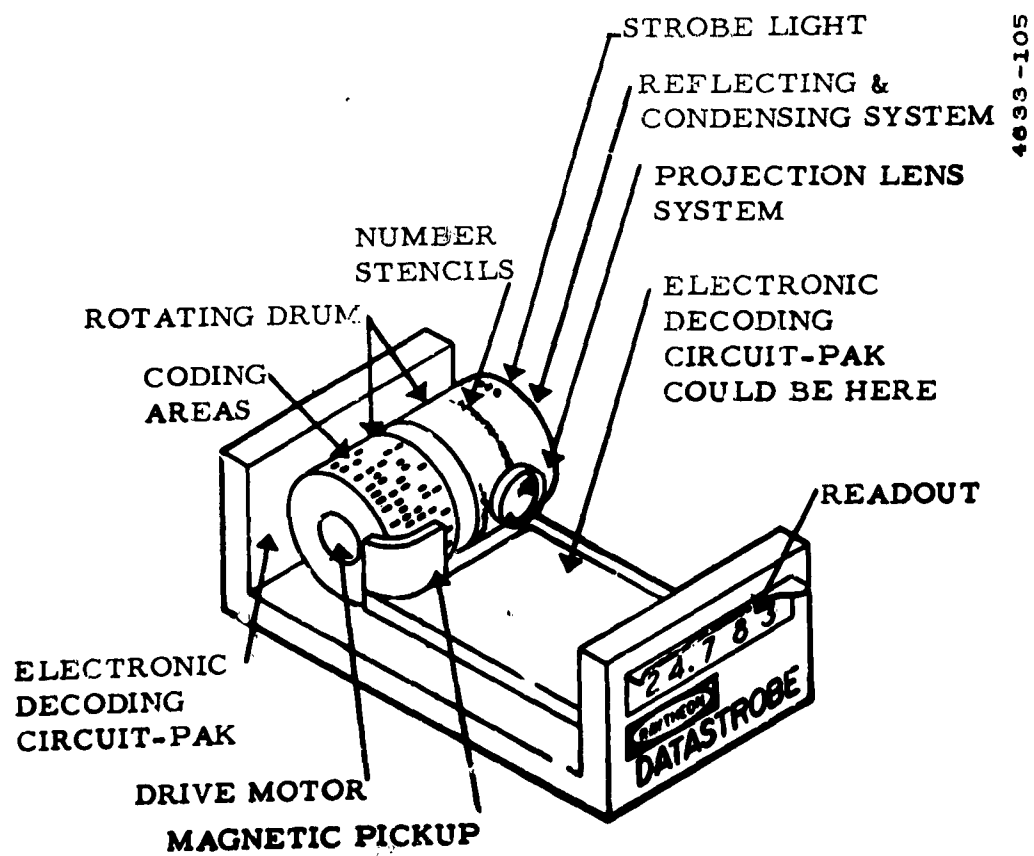
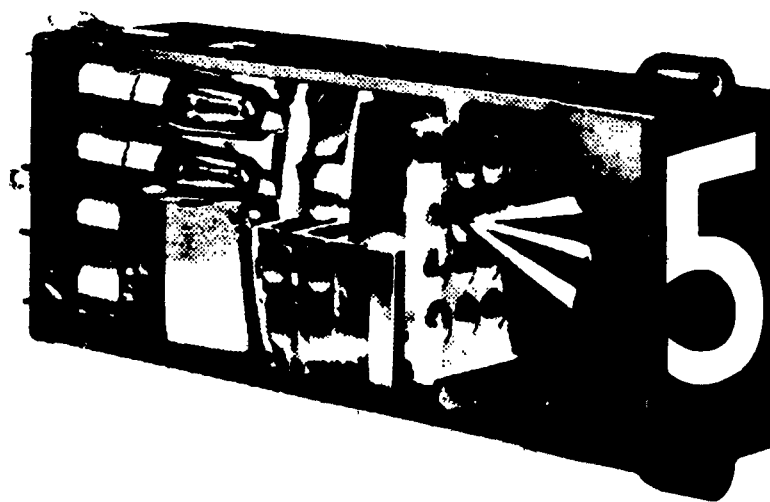


Figure 3-84. Production Model of the Datastrobe



4633-106

Figure 3-85. Transfer Device



4693-107

Figure 3-86. Projection Readout

The most widely used device of this type has a light, mask, and lens for each digit. The optical arrangement is such that each digit is projected at the same location on the viewing screen. Each mask may form any symbol, character or multicharacter message that fits the viewing screen when projected and is readable from the desired distance.

A variation of this device utilizes a single light source and lens system with movable masks. Character selection is performed by a mechanical device which positions the desired mask in the projection position. One indicator uses a D'Arsonval meter movement as a positioning device.

Another method uses a single lamp and lens with a stack of plates (one for each character up to approximately 40). This leaves hole patterns punched in such a way that light passes over all except the selected plate which then controls the cross-section of the transmitted light beam. The character is formed on the viewing screen by a large number of closely spaced dots. The character plates are controlled by a set of supporting bars raised and lowered as a function of the binary input code. Coding notches on the edges of the plates permit only the selected plate to drop into the viewing position.

A somewhat similar device uses a stepping motor controlled by a digital input code to position the character forming matrix. This device could also be classified as electromechanical. The seven segment pattern for displaying digits is also applied to a light transfer device with a separate light controlled to light each segment. As with the projection devices, all digits are displayed on the same plane, thus permitting viewing over a large range of angles.

Light transfer devices, in general, supply good visibility and legibility over a wide range of ambient light levels. The response time is about an order of magnitude less than the electromagnetic units. The use of incandescent lamps is the major factor affecting reliability.

A very important consideration with most of these devices is that they have no inherent memory. Thus, external memory must be provided for each display element, such as each lamp in multiple lamp units or each mask position for movable mask unit. The type of movable mask unit with coded character plates has, however, the same memory by inertia or latch that is characteristic of electromechanical displays.

Light-Emission Devices

In this type of device, the character is formed directly by a light emitting element either as a complete character or in selected segment form. The processes used in producing these displays fall into three general classifications: (1) Cold cathode ion discharge - - luminosity of an ionized gas, (2) electroluminescence - - direct conversion from electrical input to light within suitable phosphors, (3) Secondary emission-photon emission by electron bombardment of a phosphor-coated screen.

Glow discharge devices are generally made in the form of glass envelopes with a pin base. Electroluminescent units are normally made as flat panels. Secondary emission devices characterize cathode ray tubes and are made in such a variety of sizes and types that they are considered as a separate class (see sub-section 3.2 on CRT's - storage types).

1. Cathode Glow Devices

These devices are made in three types: (1) position indicator, (2) shaped cathode, (3) segmented matrix.

This type of indicator is normally used in counting devices. The position indicator does not form a character directly, but by means of an illuminated dot indicates which of the characters on a surrounding bezel has been selected. A glow is formed around the selected cathode.

The most common type of cathode glow device utilizes a stack of shaped cathodes and an anode (see Figures 3-37 and 3-88). When the selected cathode is made sufficiently negative with respect to the anode it glows and the resultant character representation is seen through the glass envelope. The mechanical configuration may be arranged either for viewing the device "end-on" or from the side. The stacked elements result in a decrease in the viewing angle as in the edge lighted display.

There are two basic variations of this device. One has ten cathodes and a single anode and is commonly known as a "nixie". The other has two anodes, the five odd numbered cathodes are grouped with one anode and the even numbers with the other anode.






TUBE GROUP	MINATURE	STANDARD	SUPER	LARGE	JUMBO
					
NUMERAL SIZE HEIGHT	0.3"	0.6"	0.8"	1.375"	2.0"
MAXIMUM VIEWING DISTANCE	11-14 FEET	27-30 FEET	37-38 FEET	60-65 FEET	90-100 FEET

Figure 3-87. Gas-Discharge Readout

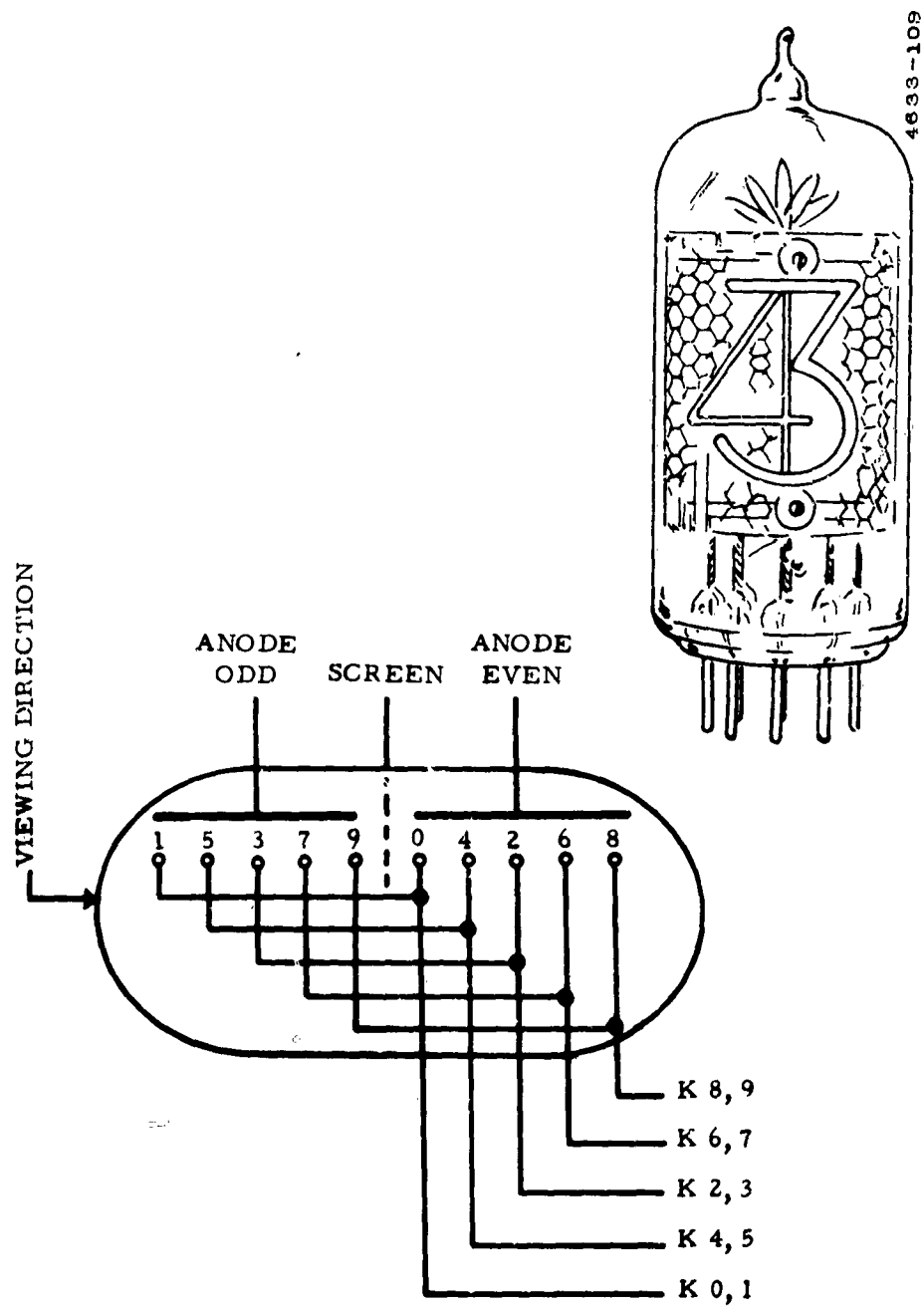


Figure 3-88. Side-Viewing Gas-Discharge Readout

This device is known as a biquinary tube. This arrangement of elements permits a reduction in the number of high voltage transistors required for control purposes.

Another cathode glow device utilizes a series of thin glow tubes, which are arranged to form characters in segmented line form. Most often, seven segments for numerics and 13 segments for alpha numerics are used. This device has the usual advantage of a single plane display, i. e., readability over a wide observation angle.

The cathode glow devices do not have inherent memory, and hence memory must be incorporated into the control circuits.

2. Electroluminescent Digital-Display Devices

These devices are basically capacitors with phosphorous imbedded in the dielectric. The phosphors are excited by alternating current flowing in the dielectric. At least one of the capacitor plates is transparent to permit viewing of the emitted light. Shaping of one of the capacitor plates controls the form of the emitted light pattern. Typical construction of an electroluminescent device is illustrated in Figure 3-89.

The brightness is related both to applied voltage and frequency as illustrated in the typical characteristic curves (for more details, see section on Electroluminescents).

The most common electroluminescent display devices are of the segmented character type with 8 to 10 segments for numerics and 12 to 16 segments for alphanumerics.

These electroluminescent devices have no inherent memory hence external memory and control must be provided. One scheme of providing memory combines a photo-conductive device with the electroluminescent elements to provide a latching action and make the light source part of the memory.

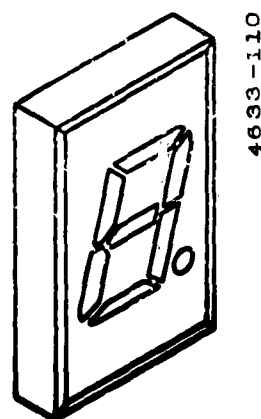


Figure 3-89. EL Readout

IV CONCLUSION

The state of the art in computers and displays/controls has been reviewed and research trends assessed. With reference to computers, the emphasis is on "batch technology processes" both for logic and memory. In the logic area, bulk silicon monolithic technology has a large lead over thin-film technology and to our best judgment, will maintain this through the 1973-78 era. This technology will also spawn more sophisticated computer organizations because of the economy with which complex logic structures will be fabricated and packaged. One direction such computer organizations may take is the block-oriented type with each computer having an array of processors available to it. Advantages of this organization include an order-of-magnitude increase in computing speed and an inherent analog-type I/O system, i. e., delay is virtually eliminated in the acceptance and transmittance of data. Where long mission times are concerned, a likely trend will be an increased redundancy and voting at the elemental logic level. The previous prohibitive cost of this approach will be overcome with the introduction of logic arrays containing several hundred to one thousand active elements.

With respect to memory technology, here, too, thin-film techniques seem to be losing out to other monolithic ferrite technologies. The chief disadvantages of the films have been low signal level (1-2 mv), high driving-current requirements, and a not-impressive packing density. Monolithic ferrite techniques currently in development include the laminated ferrite, the "waffle iron," the "flute," and the post and film. Not to be overlooked in the near term is the continuing improvement in core technologies. Small developmental memories using cores with 7.5 mils ID, 12.5 mils OD, were demonstrated late in 1965. Likewise, multi-aperture devices for NDRO use such as BIAX have been greatly reduced in size. Finally in the 1973-78 time-frame there is an excellent chance that semiconductor memories (MOS type) will be in use. Thus it is evident that the technology which gains ascendancy in the memory area must not only demonstrate technical superiority, but also have a wide margin of economic superiority--or in the current jargon, have superior cost-effectiveness.

The projection of computer technology is made in Table IV-1. By 1970, block-oriented computers featuring MOS logic and a batch ferrite memory may be introduced. The conversion system will be decentralized on a sensor/actuator level. With respect to weight, it will be slightly more than half the 1965 central computer complex. Volume will not decrease as dramatically, since a large part of the volume is devoted to nonelectronic components. For the 1973-78 period, block oriented computers will increase in array size, enabling the computer complex to keep step with the increasing sophistication of the avionics. A 400-element computing array is forecast. Also for this time period, weight will have been reduced to slightly less than one-half that of the 1965 central computer.

With respect to displays, the projection to 1970 can be made with a good deal of certainty, whereas the 1973-78 projections are highly dependent on the results of current research. The trends to 1970 are highly evolutionary, involving CRT's in one form or another. The chief advances sought are CRT's with higher resolution and brightness, wider-angle optics for head-up displays, systems which facilitate selection from a multiplicity of sensors such as scan conversion or new, rapid-erase storage tubes, and high contrast EL panels to replace electro-mechanical and mechanical instrumentation. At this time, each of these improvements must be regarded in the development phase, with, however, an excellent chance for operational use by 1969-70. A fair chance also exists for the introduction of color, what with the current large commercial efforts to simplify color TV systems. With respect to the 1973-78 time-frame, the chief question is whether the CRT (accompanied by scan conversion or otherwise a storage tube) will be replaced by a flat, rugged, computer addressed EL display. These projections are shown in Table IV-2.

Display-system weight, volume, and power will be reduced as a result of increased use of microelectronics. More important, MTBF will be increased by threefold, leading to increased confidence and utilization of electronic displays.

TABLE IV-1
PROJECTED AVIONIC COMPUTER TECHNOLOGY

Operational Use Date:	1965	1967	1969-70	1973-78
Computer Type	Central Digital Data Processor General Purpose, Parallel Binary Arithmetic, NDRO-DRO Memory Word Length, 20-30 bits Multilevel Priority Interrupt 8000 Word Memory Indexing; Indirect Address; Clock: 1-2 mc/s	Decentralized Processor Digital Differential Analyzer (DDA) Modules; Special Purpose Modifiable Program 100-150 Integrators Core Memory Store Signal Transfer Unit (STU) Monitoring all Modules	Decentralized Processor Block Oriented Computer Organization; 10:1 increase in Compute. Speed Computing Array of 10 x 10 Size 16,000 Word Memory STU for Monitoring Redundancy & Voting in Key Reliability Areas	Centralized Processor Block Oriented Computer Organization Another 2:1 increase in Computer Speed 20 x 20 Computing Array 37,000 - 64,000 Word Memory STU for Monitoring Redundancy & Voting in Key Reliability Areas
Key Technology	Discrete Ferrite Memory, Micro-Integrated Logic Circuits, Discrete Memory Circuits	Same as '65 except MIC Memory Circuits and Initial Use of MOS	Metal Oxide Semiconductor Logic; Batch Ferrite Memory	MOS Chips with up to 1000 Elements for Logic & Memory vs. Monolithic Bipolar Silicon and Batch Ferrite Memory
Weight (lbs.)	75	50 (5 modules)	40	35
Volume (ft) ³	1.2	1.0 (5 modules)	0.8	0.7
MTBF (hours)	1000	5000	7000-10,000	10,000
Conversion System	Shaft Encoders plus Central Successive Approx. System for DC/Digital	Same except Use of Magnetic Encoders and MIC Circuits. System Partially Decentralized	Decentralized on Sensor/Actuator Level	Same, with increasing Digital Interface Compatibility between Sensors, Actuators, & Computer Complex

TABLE IV-2
PROJECTED AVIONIC DISPLAY TECHNOLOGY

Operational Use Date:	1965	1967	1969-70	1973-78
System Display Functions	Pilotage, Navigation Weapons Delivery	Same with Pilotage Augmented by Transition and Hover Rqmts.	Augmented by Reconnaissance Functions	Same
Head up Display	Bright CRT & Projection System; Mechanical Reticles	Same, with addition of Electronic Reticles & higher brightness tube	Same, with $\pm 25^\circ$ Optics (spherical lens)	Same, with possibility of transparent EL
Instruments	Round Dial	Tape	High Contrast EL Panels	EL Panels with Improved Contrast and Brightness
Multisensor	Direct View Storage	Multimode storage	High resolution flat tube CRT with Scan Conversion Adaptable to varying sensor data rates vs. rapid erase storage tubes	EL Panels vs. vs. CRT & Scan Conversion vs. Rapid Erase Storage Tube
Horizontal Situation Display	Conventional Mechanical Indicators	CRT Display; Superimposed Map; Electronic Symbol Generator; Selectable & Superimposed Video	Same, plus improved Display Tubes	Rapid Erase Storage Tube Colored Symbology
Navigation and Tactical Maps Display	Paper Maps - Hand Held	Integrated into Horizontal Situation Display	Same	Same
Physical Characteristics		Fully Electronic Display System	20% Weight Reduction thru Scan Conversion; Lower Power; Higher Display Legibility	Additional Volume Savings thru Flat EL Displays
Total System Weight (lbs.)		150	120	100
Volume (cu. in.)		6400	5200	3700-5000
Power (watts)		800	625	600
MTBF		1000	2000	3000

Security Classification

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13. ABSTRACT <p>Computers and Displays/Controls for avionics systems are discussed primarily from a technology standpoint. The current state of the art is reviewed, current research developments are pointed out and prediction of when these developments will be incorporated into avionic systems is given.</p> <p>With respect to computers, the following major categories are assessed: a) Logic, b) Memory, c) Computer Organization, d) Analog/Digital Conversion. Emphasis is placed on the impact of batch fabrication to these areas.</p> <p>With respect to Displays/Controls the following major categories are reviewed: a) CRT's, b) Scan Conversion, c) Color, d) Analog/Digital Techniques for range scaling and symbol generation, e) Electroluminescence.</p> <p>A summary chart projecting state of the art for computers and displays/controls to the 1975 period is presented at the end of the report.</p>			

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Avionics					
Logic					
Memory					
Scan Conversion					

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